7. **Low-Noise Amplifier Design**
Outline

- Low noise amplifier overview
- Tuned LNA design methodology
- Tuned LNA frequency scaling and porting
- Broadband low noise amplifier design methodology
7.1 LNA overview
Tuned LNA topologies

CB/CG (no feedback)

Cascode (L or xfmr feedback)

CS/CE (L or xfmr feedback)
**Design goal**

- Minimize the noise of the amplifier for a given signal source impedance to approach transistor minimum noise figure/factor $NF_{MIN}/F_{MIN}$

\[
F = F_{MIN} + \frac{R_n}{G_s}|Y_s - Y_{sopt}|^2
\]

- Input and output matching to source and load.

- Maximize gain ($G$) and linearity ($\text{IIP3}$)

- Reduce DC power $P_{DC}$ => conflict with $F$ and $\text{IIP3}$

\[
FoM_{LNA} = \frac{G \times \text{IIP3} \times f}{(F - 1)P_{DC}}
\]
Design philosophy

- Take advantage of what silicon does best: transistors.

- Use Si passives only sparingly:
  - Q is fairly low and undermines overall noise figure
  - Inductors are (significantly) larger than transistors, hence expensive.

- Make transistor sizing part of the noise matching step.

- Use only reactive (loss-less) feedback or minimize the noise contribution of resistive feedback components.

- Avoid active loads if at all possible.
LNA design fundamentals

- Device noise fundamentals:
  - $\text{Re}\{Z_{\text{sopt}}\} \leftrightarrow \text{Re}\{Z_{\text{IN}}\}$ and $\text{Im}\{Z_{\text{sopt}}\}$ approx. $\text{Im}\{Z_{\text{IN}}\}$ (within 15%)
  - $\text{Re}\{Z_{\text{sopt}}\} = k \frac{f_t}{(f g_m)}$
  - $F_{\text{MIN}}$ is invariant to number of gate fingers $N_f$, and number of transistors $m$ connected in parallel, but depends on $W_f$.
  - Reactive (lossless) feedback does not affect $F_{\text{MIN}}$ and $\text{Re}\{Z_{\text{sopt}}\}$
  - Power is dictated by noise impedance matching ($V_{\text{DD}} J_{\text{OPT}} f_t / g'_m$)
  - Saving power comes with the price of compromising noise and linearity!
Tuned and broadband LNA design philosophy

- Active device for noise impedance
  - Find optimal $W_f$ for given frequency
  - Bias for minimum $NF_{MIN}$ and
  - Sizing ($N_f$) for $\text{Re}\{Z_{sopt}\} = 50 \, \Omega$

- (lossless) feedback for input impedance matching $Z_{IN}$ and $\text{Im}\{Z_{sopt}\}$

All lossless feedback configurations work:
  - Series-series, shunt-series, series-shunt, shunt-shunt

Transimpedance feedback works best for broadband LNAs

\[
\frac{\partial F_{MIN}(W_f)}{\partial W_f} = 0
\]

\[
\frac{\partial F_{50}(N_f)}{\partial N_f} = 0
\]
Biasing LNA topology for minimum noise

- MOSFET, cascode $J_{OPT} = 0.15$ mA/µm irrespective of $W_f$, node, and frequency

- Lowest current for optimally biased MOS-LNA is 150µA for single 1µm finger

- In HBTs $J_{OPT}$ varies with frequency, topology, and technology node
Sizing the MOSFET/HBT (cascode) for $R_{SOPT}$

FET/HBT (casc) biased at $J_{opt}$

Noise parameters scale with $(l_E)N_f$ for fixed $W_f$.

\[ \Re[Z_{sopt}(N_f, f)] = Z_0 \] coincides with \[ \frac{\partial F_{50}(N_f)}{\partial N_f} = 0 \]

\[ \Re[Z_{sopt}(l_E, f)] = Z_0 \] coincides with \[ \frac{\partial F_{50}(l_E)}{\partial l_E} = 0 \]
Sizing the FET (cascode) for $R_{SOPT}$

\[ R_n = \frac{R_{N,FET}}{N_f N} \quad G_u = G_{N,FET} \omega^2 N_f N \]

\[ G_{cor} = G_{C,FET} \omega N_f N \quad B_{cor} = B_{FET} \omega N_f N \]

\[ Y_{sopt} = \sqrt{G_{cor}^2 + \frac{G_u}{R_n} - jB_{cor}} = N N_f W_f \omega \left( \sqrt{G_{C,FET}^2 + \frac{G_{FET}}{R_{FET}} - jB_{FET}} \right) \]

\[ Z_{sopt}(FET) \approx \frac{f_{Teff}}{N \cdot N_f \cdot W_f \cdot f \cdot g'_m \cdot meff} \left[ \sqrt{\frac{g'_m \cdot R'_s + W_f \cdot g'_m \cdot R'_g(W_f)}{k_1}} \right] = Z_0 + jX_{sopt} \]

\[ N N_f = \frac{f_{Teff}}{Z_0 \cdot W_f \cdot f \cdot g'_m \cdot meff} \sqrt{\frac{g'_m \cdot R'_s + W_f \cdot g'_m \cdot R'_g(W_f)}{k_1}} \]
Sizing the HBT (cascode) for $R_{SOPT}$

$$R_n = \frac{R_{HBT}}{N I_E}$$

$$G_u = G_{HBT} \omega^2 N I_E$$

$$G_{cor} = G_{C,HBT} \omega N I_E$$

$$B_{cor} = B_{HBT} \omega N I_E$$

$$Y_{sopt} = \sqrt{G_{cor}^2 + \frac{G_u}{R_n} - jB_{cor}} N I_E \omega \left( \sqrt{G_{C,HBT}^2 + \frac{G_{HBT}}{R_{HBT}} - jB_{HBT}} \right)$$

$$Z_{sopt}(HBT) \approx \frac{f_{Teff}}{f \cdot N \cdot I_E \cdot g_{meff}} \left[ \sqrt{\frac{g_m}{2}} (r'_E + R'_b) + j \right] = Z_0 + jX_{sopt}$$

$$N I_E = \frac{f_{Teff}}{Z_0 \cdot f \cdot g_{meff}} \sqrt{\frac{g_m}{2}} (r'_E + R'_b)$$
RF CMOS/HBT LNA design equations

\[ \Re [Z_{\text{sopt}}(N_f(I_E), f)] = Z_0 \] coincides with \[ \frac{\partial F_{50}(N_f(I_E))}{\partial N_f(I_E)} = 0 \]

\[ L_S = \frac{Z_0 - R_s - R_g}{\omega_T \text{(cascode)}} \]

\[ L_S = \frac{Z_0 - R_b - r_E}{\omega_T \text{(cascode)}} \]

\[ Z_{\text{IN}} = \omega_T L_S + R_g + R_s + j \left[ \omega (L_S + L_G) - \frac{f_T}{f g_m} \right] \]

\[ Z_{\text{IN}} = \omega_T L_S + R_b + r_E + j \left[ \omega (L_S + L_G) - \frac{f_T}{f g_m} \right] \]

\[ L_G = \frac{f_T}{2 \pi f^2 g_m} - L_S \]

\[ G \leq \frac{1}{4} \frac{f_T^2 R_P}{f^2 Z_0} \]
Refinements for mm-waves: S. Nicolson (CSICS-06) 

(i) Source Impedance

- With bondwire
  \[ R_S = n \times Z_0; \]
  \[ R_S = \frac{Z_0}{(1 - \omega^2 L_{BW} C_{PAD}) + \omega^2 Z_0^2 C_{PAD}^2}; \]
  \[ X_S = j \omega \frac{L_{BW}(1 - \omega^2 L_{BW} C_{PAD}) - Z_0^2 C_{PAD}}{(1 - \omega^2 L_{BW} C_{PAD}) + \omega^2 Z_0^2 C_{PAD}^2}; \]

- Without bondwire
  \[ R_S = \frac{Z_0}{k}; \]
  \[ Z_S = \frac{Z_0}{k} - j \frac{\omega C_{PAD} Z_0^2}{k}; \]
  \[ k = 1 + \omega^2 C_{PAD} Z_0^2; \]
Refinements for mm-wave CMOS LNAs: (ii) $f_T$ of topology with $L_M$ after extraction

$L_{M1}$ forms artificial t-line with parasitics of $M_1$ and $M_2$. An optimal $L_{M1}$ exists that maximized $f_T$.

$$L_{M1} \sim W_1^{-1}$$

Both the gain and the noise figure are improved.

$$f_T(\text{cascode}) = \frac{g_{m1}}{2\pi(C_{gs1}+2C_{gd1})}$$
Calculate effective source imp. \( Z_S = R + jX_S \)

Find optimal \( W_f (I_E) \) and bias at \( J_{OPT} \)

Find \( L_{M1} \) which maximizes \( f_T \) of topology @ \( J_{OPT} \)

Find \( N_f \) such that \( R = \text{Re}(Z_{SOPT}) \) @ \( J_{OPT} \)

Find \( L_S = R/\omega_T \) such that \( R = \text{Re}(Z_{IN}) \)

Find \( L_G \) such \( X_S = \text{Imag}(Z_{IN}) = \text{Imag}(Z_{SOPT}) \)

Design output matching network: \( L_D, C_D \) for maximum gain
Examples: SiGe HBT vs. 90-nm CMOS Cascode LNAs

- **RF IN**
  - $L_1 = 90 \, \text{pH}$
  - $L_2 = 60 \, \text{pH}$
  - $J_{C1} = 4.2 \, \text{mA}$
  - $J_{C2} = 6.7 \, \text{mA}$
  - $C_c = 23 \, \text{fF}$
  - $L_{PRI/SEC} = 160 \, \text{pH}$

- **RF OUT-DIFF**
  - $R_{C2} = 1 \, \text{k}\Omega$
  - $L_C = 120 \, \text{pH}$

- **RF OUT**
  - $L_{b2} = 110 \, \text{pH}$
  - $C_{c2} = 100 \, \text{fF}$
  - $L_{b1} = 70 \, \text{pH}$

- **Dimensions:**
  - **RF IN**: 370 µm
  - **RF OUT-DIFF**: 480 µm
  - **RF OUT**: 350 µm

- **Parameters:**
  - $V_{cc} = 3.3 \, \text{V}$
  - $V_{dd} = 1.5 \, \text{V}$
  - $V_g = \text{Supply}$

- **Currents:**
  - $J_{C1} = 4.2 \, \text{mA}$
  - $J_{C2} = 6.7 \, \text{mA}$
  - $I_{D1} = 70 \, \text{pH}$
  - $I_{D2} = 90 \, \text{pH}$
  - $I_{m1} = 70 \, \text{pH}$
  - $I_{m2} = 90 \, \text{pH}$

- **Capacitance:**
  - $C_{c1} = 150 \, \text{fF}$
  - $C_{c2} = 100 \, \text{fF}$
Ac-coupled cascode, 1V operation in GP CMOS, insensitive to $V_T$, yet:

- 2x the DC current
- 2nd resonant tank reduces bandwidth,
- extra lossy inductor and MIM cap => higher loss, larger area
140-GHz 65-nm CMOS LNA

6-stage AC-coupled cascode amplifier
- 63 mW at 1.2V
- 20% stage scaling
- 300μm x 500μm inc. pads

[S. Nicolson RFIC-08]
Measured S-params and linearity
LNA bias network

- Reference current may come from bandgap circuit
- Base resistance should not allow for >2mV drop
- Transistors must be in close proximity in layout.
- $V_{CE}(Q_2)$ should be large for large IIP3
Bias circuits (ii)
Bias circuits (iii)
Differential noise matching

- Design differential half-circuit to be matched to $Z_{\text{sopt}}$ (50$\Omega$)

- $Z_{\text{soptdiff}} = 2Z_{\text{sopt}} (Q_1) + 2j\omega (L_E + L_B)$

- $Z_{\text{INdiff}} = 2\omega L_E$
MOSFET LNA design usually compromises noise figure for power dissipation (low-noise current is too high!)

- In this approach linearity increases with $Z_o$.
- Pad capacitance and parasitic capacitance of $L_B$ reduce input impedance.
- Tail current source in diff-pair adds noise and common-mode instability. Not recommended!
Tuned LNA topologies summary

CS/CE (L or xfmr feedback)
- low-voltage, low-noise, good linearity,
- poor isolation => difficult to separately design input/output network

CB/CG (no feedback)
- moderate noise, good isolation (HBT-only)
- poor linearity, difficult to simultaneously match noise and source impedance

Cascode (L or xfmr feedback)
- best isolation, low-to-moderate noise, easy to match, good linearity
- higher supply voltage (but available due to mixer)
Frequency scaling of CMOS LNAs

- **Goal**: Scale the LNA centre frequency
  \[ f_0' = \alpha f_0 \]

- **Step 1: Biasing for Minimum Noise**
  - \( J_{\text{OPT}} \) unchanged @ 0.15mA/\mu m

- **Step 2: Device Sizing**
  - \( W_F \) unchanged

\[ N_F' = N_F / \alpha \]
\[ W' = W / \alpha \]
Frequency scaling of CMOS LNAs (ii)

- **Step 3: Input Impedance Matching**
  - $L_S$: unchanged
  - $L_G$: $L'_G = L_G / \alpha$

  \[
  L'_G = \frac{1}{(\alpha \omega)^2 \left( \frac{C_{IN}}{\alpha} \right)} - L_S
  \]

- **Step 4: Output matching**

  $L'_D = L_D / \alpha$
  $C'_1 = C_1 / \alpha$
  $C'_2 = C_2 / \alpha$
### Experimental results

<table>
<thead>
<tr>
<th>LNA</th>
<th>$N_f$</th>
<th>$W_f$</th>
<th>$I_{DS}$ mA</th>
<th>$V_{DD}$ [V]</th>
<th>$L_S$ [pH]</th>
<th>$L_G$ [pH]</th>
<th>$L_D$ pH</th>
<th>$L_M$ pH</th>
<th>$C_1$ [fF]</th>
<th>$C_2$ [fF]</th>
<th>$C_{PAD}$ [fF]</th>
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<tr>
<td>14 GHz, 90-nm</td>
<td>90</td>
<td>1</td>
<td>13.5</td>
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<td>128</td>
<td>1100</td>
<td>545</td>
<td>-</td>
<td>145</td>
<td>70</td>
<td>20</td>
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<td>6.75</td>
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<td>75</td>
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<td>60 GHz, 90-nm</td>
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<td>3</td>
<td>1.5</td>
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<td>190</td>
<td>140</td>
<td>190</td>
<td>30</td>
<td>-</td>
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</tr>
<tr>
<td>12 GHz, 130-nm</td>
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<td>13.5</td>
<td>1.8</td>
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<td>-</td>
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<td>24 GHz, 130-nm</td>
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<td>6.75</td>
<td>1.8</td>
<td>177</td>
<td>718</td>
<td>251</td>
<td>-</td>
<td>80</td>
<td>58</td>
<td>60</td>
</tr>
</tbody>
</table>
Frequency scaling of 90-nm CMOS LNAs

- Scaling error less than 8%
- Typical process variation: ~20%!
Design porting of CMOS LNAs

- **Goal**: Keep center frequency unchanged, port LNA to another technology node

- **Step 1: Biasing for Minimum Noise**
  - Unchanged: $J_{\text{OPT}}$ is invariant between technology nodes

- **Step 2: Device Sizing**
  - Unchanged: $Z_{\text{OPT}}$ is invariant between technology nodes

\[ W'_{f} = \frac{W_{f}}{S} \quad \Rightarrow \quad W' = W \]

\[ N'_{f} = N_{f} \times S \]
Design porting of CMOS LNAs (ii)

• Step 3: Input Matching

  – $L_S$ roughly scaled by $1/f_T$:
    $$L_S = \frac{Z_0 - R_g - R_s}{2 \pi f_T}$$

  – $R_G + R_S$ remains approximately constant if $W_f \Rightarrow W_f/S$ and $W=ct.$

  – $L_S + L_G$ unchanged because transistor size unchanged
Benefits of scaling for RF/mm-wave

Gain and NF improve with scaling
Power-constrained LNA design

**Problem**: GHz-range, noise-matched CMOS LNAs consume significant power

**Solutions**
- Current re-use with CMOS inverter (doubles $V_{DD}$ but still saves power)
- Don't noise match, just bias at $J_{opt}$
- Use external capacitor between gate and source: degrades both gain and NF

\[
\begin{align*}
    f_T & \rightarrow \frac{f_T}{C_1} \\
    L_S & \rightarrow L_S \left(1 + \frac{C_1}{C_{gs} + 2 C_{gd}}\right)
\end{align*}
\]
Lossless series-series feedback noise matching scheme

- Pad capacitance causes second, parallel resonance
- Series and parallel resonance reduce input impedance matching bandwidth
- \( \frac{R_{\text{sopt}}}{G_{\text{sopt}}} \) is frequency dependent, so noise matching is NOT broadband
(Lossy) Shunt-series feedback reduces optimal noise impedance

- Single resonance increases input impedance matching BW
- Reduces the transistor size & current for noise matching
- The noise matching is still narrow band because $G_{SOPT}$ is frequency-dependent
Ex.: W-Band LNA with xfmr feedback
Other low-noise amplifier concepts

• “Noise cancellation” idea by Bruccoleri et al. ISSCC-02
• CG for impedance matching and TIA/ CS for noise matching
• They don't cancel noise, they achieve noise matching over broader bandwidth
Tuned, narrow-band LNA summary

- Cascode with inductive degeneration is the most common topology for LNAs
- Algorithmic design methodology for MOS and HBT LNAs up to 90 GHz
- In MOSFETs $J_{OPT}$ & $Z_{OPT}$ invariant between nodes
- CMOS LNA design scalable in frequency and portable between nodes without redesign
- Frequency scaling error <8%
Back-up slides
7.2 Tuned LNA design methodology using a simulator
Cascode topology with series inductive feedback

- Good isolation allows for separate input/output matching network design.
- Bias current is shared resulting in low power.
- Limited to about 1.8V supply (HBT) or 1.2V supply (LVT MOSFETs)
- Noise slightly degraded (compared to CE/CS) by common base (gate) device.
- If common base/gate device is sized for max. speed, $\text{NF}_{\text{min}}$ is degraded by a few tenths of dB.
**Tuned LNA design steps**

- Set $V_{CE}/V_{DS}$ on transistor to maximize linearity (avoid output clipping as in PA design)
- Bias transistor @ minimum NF current density;
- Size transistor for optimal noise resistance - *active device matching*;
- Add passive (inductive) components for optimal noise impedance, input/output impedance and gain - *passive device (classical) matching*;
- Add base/gate bias circuitry without impact on noise;
- If linearity goal is not met (typically because of transfer characteristics) use gain control schemes or increase size or current density (may change input matching)
Step 1: find the $J_{opt}$ for the HBT cascode

At low-noise bias read $f_T$; use average initial size $l_E = 5 \, \mu m$ and 2 emitter, 3 base, 2 col. HBT
Step1b: HBT cascode low-noise bias (read $J_{opt}$)
Step-2: cascode sizing for $\text{Re}(Z_{\text{sopt}}) = Z_0$
Step 3a: add $L_E$ such that $\text{Re}(Z_{IN}) = Z_O$

$$L_E = \frac{Z_O - R_b - R_E}{2\pi f_T(\text{cascode})}$$
Step 3b: add $L_B$ such that $\text{Im}(Z_{\text{IN}}, Z_{\text{sopt}}) = 0$

\[
Z_{\text{IN}} \approx Z_O + j \omega (L_B + L_E) + \frac{1}{j \omega C_{\text{in}}}
\]

\[
L_B \approx \frac{1}{\omega^2 C_{\text{in}}} - L_E
\]

\[
Z_{\text{SOPT}} = Z_O
\]

\[
Z_{\text{IN}} = Z_O
\]
Step 3c: add $L_C$ for maximum gain

- $L_C$ should be as large as possible for gain
- $C_C$ helps lower impedance
- May use 3-terminal inductor or transformer for impedance transform to $Z_o$
- Linearity is maximized by setting:
  $$R_{CTank} \times I_{copt} = V_{CE}(Q2) - V_{CESAT}$$
- $R_{CTank}$ is the equiv. parallel ac resistance at the output node
Step 3d: matching the output

- Use the Smith chart with the series-shunt or shunt-series technique
- Make sure not to short-ckt. the output to ground (use shunt inductor to $V_{CC}$, not to GND.
- Use 2pF ... 5pF (depending on LNA freq) to de-couple cascode bias and $V_{CC}$ to AC ground.

$$G \leq \frac{1}{4} \frac{f_T^2}{f^2} \frac{R_P}{Z_{in}}$$