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An Application of High-Resolution Dual-Lens Dark-Field Electron Holography in Strain Analysis for Nanometer Semiconductor Device in Wafer-foundries

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Constantly striving for miniaturization of semiconductor device with nanometer transistors as the basic building block is the theme of efforts in wafer-foundries [1~7]. To synchronize with the device shrinkage, novel techniques to enhance carrier mobility within constrained geometry are developed. Several techniques can be realistically applied in the strain-engineering for Si-based nanometer transistors [4~7]. For example, SiGe, as a stressor, is introduced in p-type transistors [4]. Since a nanometer transistor device is basically a nanometer-scale composite, to effectively understand appropriate levels and desired distributions of strains applied into nanometer transistor devices is a big challenge to process integration, device characterizations, and physical failure analysis (PFA) teams.

Dark-field electron holography acquired by a Lorentz lens or a mini-condenser lens has been employed to characterize strain measurement. However, fundamentally there are two intrinsic limitations for the conventional industrial approach. One is the limited fringe spacing (e.g., 5~6nm), which is acceptable to device for 20nm or above, especially for a “planar” transistor built on bulk-Si substrate or Si-on-insulator (SOI), but hard to extend to FinFET with a Fin dimension of 14nm or below. Another obstacle was extremely time-consuming to tilt to the desired crystal zone under a typical two-beam electron diffraction condition.

Yun-yu Wang’s innovations [5~7] overcome these technical barriers. By introducing a dual lens setting with combined contributions of Lorentz lens and objective lens with various suitable strengths in a modern Analytical TEM, Wang’s pioneer work not only extends the fringe spacing to a higher-resolution (e.g., 0.5nm) range, but also enables large zone-tilt at high objective lens currents as a routine. Collectively, these two innovative settings open a door to extend dark field electron holography for strain measurement at a high spatial resolution into the era of FinFET, 14nm or even below.

One example demonstrated here is an application of Wang’s patented method in a strain characterization on an enhancement of device performance by applying SiGe into p-FET device. Key parameters achieved on a Cs image corrected Titan at Fab 8, by the dual lens electron holography aforementioned, include: (1) fringe width: 219 nm; (2) fringe spacing: up to 0.4 nm; (3) fringe contrast: over 20% ; (4) dark field holography on a 28LPQ test device to obtain strain map of <220> and <004> diffractions; and (5) level of strains, measured at top of Si: -1.6%, and 0.8%, for <220> and <004>, respectively. Clearly, strains indeed had been applied into the desired p-FET transistor gate channel. Figure-1a summarizes fringe spacing that can be accomplished versus strength of objective lens. Figure-1b displays an empty test hologram in vacuum, with fringe spacing of 0.6nm and fringe contrast of 24% (Fig-1c). Figure-1d is the device with strain in transistor gate analyzed in Figs-2 & -3. Figures-2a~2d are the dark-field electron hologram on <220> and <400> diffractions, respectively, on a device with SiGe embedded in Si-substrate. Figures 3a~3d are corresponding post-processed strain maps and extracted profiles.

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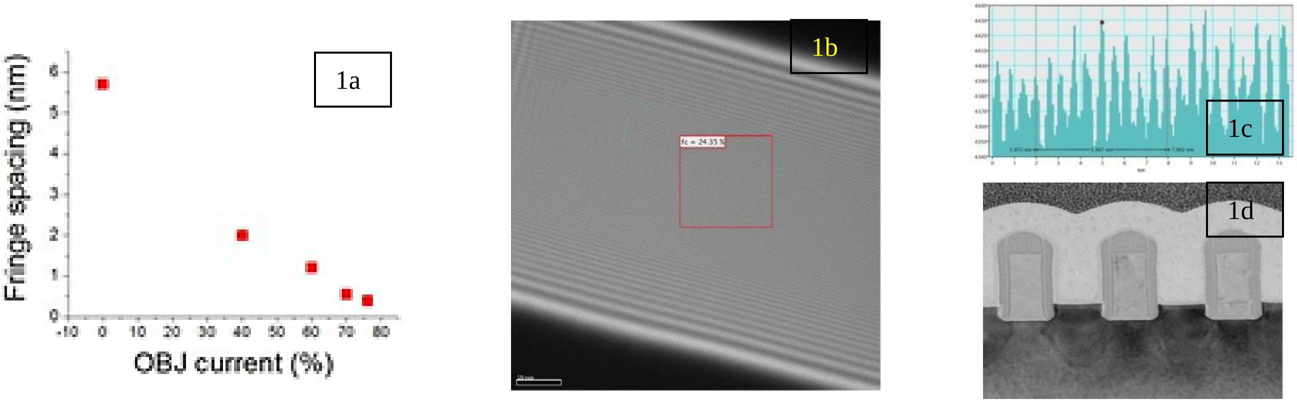

Figure 1. (a) fringe spacing vs. objective lens current; (b) and (c) a high-resolution electron hologram in vacuum, and (d) the device with SiGe stressor, with strains analyzed in Figures-2 and Figures-3.

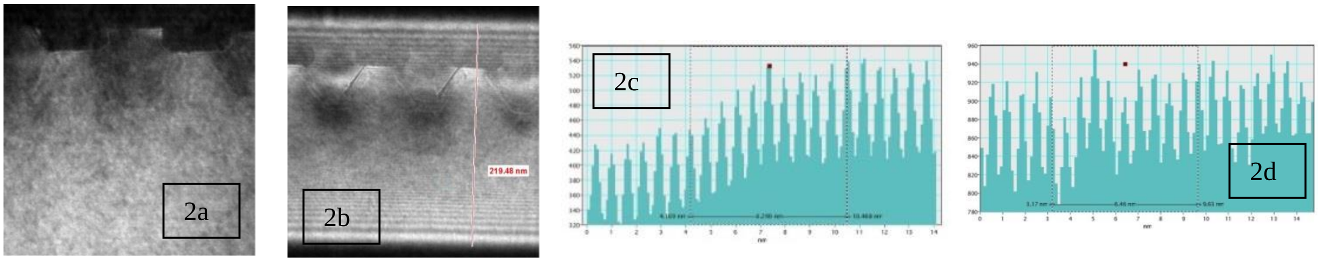

Figure 2. Dark-field electron holograms, (a) and (b), on <220> and <004> diffraction, respectively; and the corresponding proof of high-resolution fringe spacing, (c) and (d); for the device in Figure-1d.

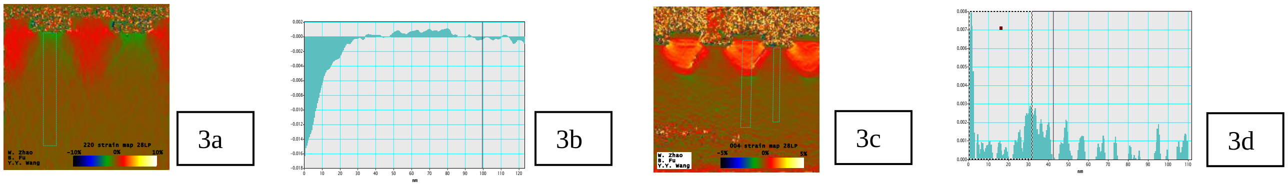

Figure 3. Post-processed strain mapping (a and c); and extracted profiles (b and d), on <220> and <004>, respectively.