EXTRINSIC PERFORMANCE LIMITATIONS OF AlGaN/GaN HETEROSTRUCTURE FIELD EFFECT TRANSISTORS

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ABSTRACT

Extrinsic effects on the DC output characteristics of AlGaN/GaN HFETs with 1μm gate lengths are examined. The devices investigated were fabricated on MOCVD-grown AlGaN/GaN heterostructures on sapphire substrates. An analytical model that takes into account parasitic resistances and thermal effects is constructed, and its results are compared with experimental data. With parameters determined from characterization experiments on the same wafer and from independent theoretical results, the agreement between the data and the model predictions is found to be very good. The model is then applied to performance predictions for devices with improved series resistances and heat sinking.

INTRODUCTION

The group III-nitride compound semiconductors have considerable potential for the fabrication of high frequency/high power electronic devices. Progress in the growth and process technology of these materials has recently led to the demonstration of very impressive results for the output current density, the gain cut-off frequency, and the output power density of AlGaN/GaN heterostructure field effect transistors (HFETs).[1,2,3] These encouraging results notwithstanding, the device design and the fabrication techniques are still far from optimized. For example, contact resistances are relatively large (compared to conventional III-V materials) and deleterious thermal effects are likely to limit the performance of the HFETs at high voltages and currents. This is particularly the case for devices fabricated on sapphire substrates, due to that material's relatively low thermal conductivity.

In this communication extrinsic effects that limit the performance of AlGaN/GaN HFETs are examined in the framework of an analytical model. The results are compared with experimental data from AlGaN/GaN HFETs. It is found that significant improvements in output current can be expected if the heat generated in the devices is removed effectively (for example by a flip-chip bonding technique, or by the use of a substrate with high thermal conductivity) and if the source and drain series resistances can be reduced.

DEVICE STRUCTURE

The III-nitrides used in this study were grown by MOCVD on sapphire substrates. The

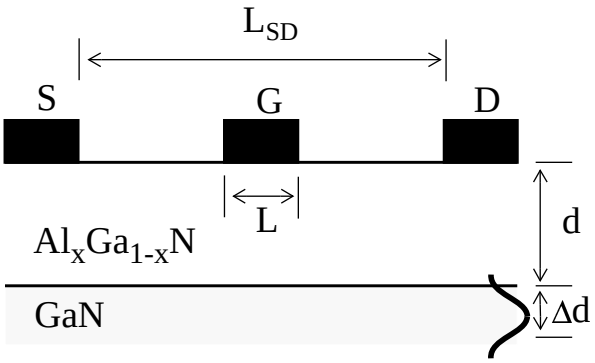

Figure 1: Schematic HFET diagram.

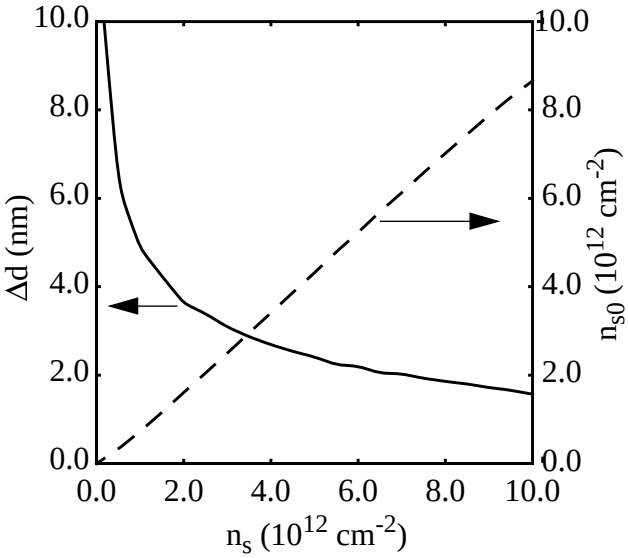

Figure 2: Calculated values of Δd and electron concentration in the lowest subband as a function of the total sheet carrier density.

material structure consisted of an AlN nucleation layer, followed by 3μm of undoped GaN and 200Å of nominally undoped $Al_{0.3}Ga_{0.7}N$. Ohmic contacts were formed using alloyed Ti/Al/Ni/Au, and the gate metallization was Pt/Au. Device isolation was accomplished through the use ECR dry etching. The source-to-drain spacing was 5μm and the gate length was 1μm. A schematic diagram of the HFETs is shown in Figure 1. The devices tested consist of two parallel gated channels of 75μm width, for a total gate width of 150μm.

DEVICE MODEL AND KEY PARAMETERS

The device model developed for this investigation is a charge-control/gradual-channel approximation model [4] that incorporates salient results of previous Monte Carlo electron transport simulations for GaN as a function of the ambient temperature.[5] A good approximation for the relationship between the channel carrier concentration, n_s, and the gate voltage is a critical prerequisite for an accurate charge-control model. Therefore, as an initial step, the capacitance vs. voltage characteristic (C-V) of the AlGaN/GaN layer structure is examined. A standard approximation that should be monitored closely is to evaluate the capacitance per unit area as $C = \varepsilon/(d + \Delta d)$ where d is the thickness of the barrier (AlGaN) layer and Δd is the effective thickness of the two-dimensional electron gas that forms the channel.[6] Clearly, the approximation of treating Δd as a constant, independent of the carrier concentration, is rather rough. This is seen immediately from a self-consistent solution of the coupled Schroedinger and Poisson equations.[7,8] By calculating the quasi-two-dimensional subband structure in this way and subsequently estimating the effective thickness as

$$\Delta d = \frac{1}{n_s}\int z n(z) dz \qquad (1)$$

the result shown in Figure 2 is obtained. Here n(z) is the total (three-dimensional) free electron density which is related to the (two-dimensional) channel carrier density by $n_s = \int n(z) dz$. The effective mass subband structure calculations are done using a self-consistent potential in the framework of the local density approximation. Also taken into account is the polarization charge at the interface that arises from the piezoelectric effect in the strained AlGaN barrier layer. At room temperature only the lowest three subbands are found to be significantly populated. The carrier density in the lowest subband which accounts for more than 80% of the

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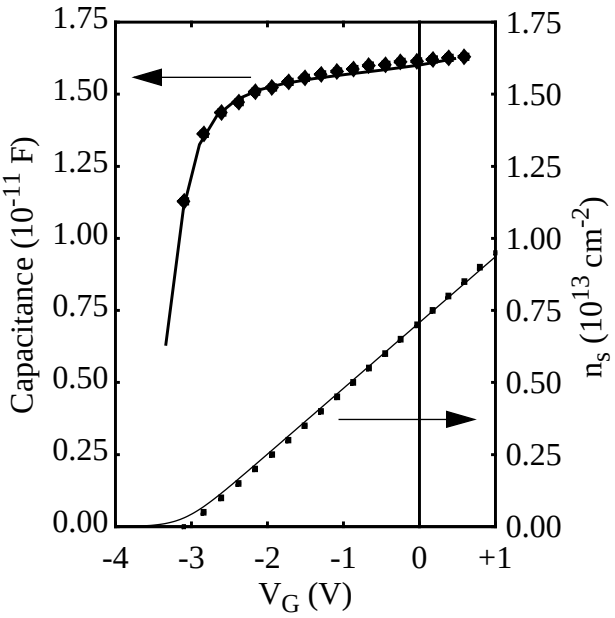

Figure 3: Comparison of the measured AlGaN/GaN heterostructure capacitance for a 75μm dot with calculated results. Also shown is the resulting n_s vs. V_g from the subband calculation (dots) and from equation (2).

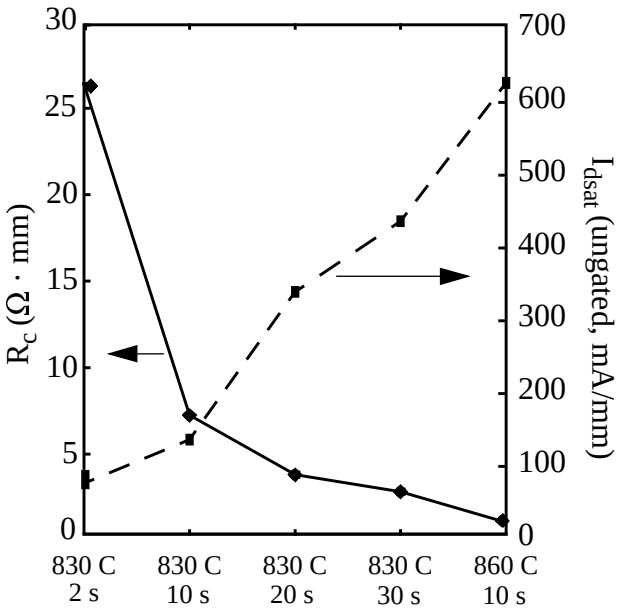

Figure 4: Measured (TLM) contact resistances and I_{dsat} for an ungated device for various anneal times and temperatures.

total is also shown in Figure 2. As is evident from the figure, Δd varies quite strongly with n_s.

From $dn_s/dV = C/q$ and $C(n_s) = \varepsilon/(d + \Delta d(n_s))$ the capacitance per unit area as a function of the gate voltage can be found by eliminating n_s. Comparing the calculated capacitance with experimental data for dot-shaped capacitors with 75μm diameter yields the agreement shown in Figure 3. While this result is very satisfactory from a point of view that focuses on the quantum confinement, it does not provide a convenient closed-form expression that can be used in a charge-control model. However, the following analytic relationship between the channel carrier concentration and the gate-to-channel voltage, V_g, accounts well for the integrated C-V data.

$$n_s(V_g, T) = MkT\log\left(\exp\left((V_g - V_t)\frac{1}{qMkT}\frac{\varepsilon}{(d + \Delta d)}\right) + 1\right) \qquad (2)$$

Here M is an effective two-dimensional density of states, and the remaining symbols have their usual meanings. The good agreement between the simple expression (2) and the result of the self-consistent solution of the subband structure problem is shown in Figure 3.

For the analytic calculation of the drain current in the HFET, the relationship between the electron drift velocity, v, and the longitudinal electric field, E, is approximated as:

$$v(E, T) = \begin{cases} \dfrac{\mu(T)E}{1 + E/(E_1(T))} & E < E_c(T) \\ v_{sat}(T) & E \geq E_c(T) \end{cases} \qquad (3)$$

where μ(T) is the low field mobility and $E_1(T) = E_c/(\mu E_c/v_{sat} - 1)$.

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The low field mobility, the saturation (peak) velocity, and the saturation (peak) field results of Monte Carlo simulations for electron transport in GaN have been parameterized as functions of temperature, doping concentration, and compensation.[5] These results are used in the present model, and the simple expression above is found to approximate the velocity vs. field curve quite well for $E \leq E_c$. The GaN channel is taken to be undoped, yielding [5] a low-field room temperature mobility of $1200 cm^2V^{-1}sec^{-1}$. This value is somewhat larger than measured Hall mobilities for the particular device structures for which we compare the model results to experimental data (typical values are $1100 cm^2V^{-1}sec^{-1}$ for $n_s = 9x10^{12} cm^{-2}$). Hence, the mobility is reduced by a small, temperature independent correction using Matthiessen's rule.

The analytic expressions for the drain current, I_d, as a function of the intrinsic gate and drain voltages, V_g and V_d, for the so-called linear and saturation regimes were presented in ref. [4]. The gate current is negligibly small for the operating conditions to be examined here.

In the present effort of accounting for the output DC characteristics of AlGaN/GaN HFETs, two extrinsic effects are included in the model. The first is the additional voltage drop across the source and drain series resistances, R_s and R_d, which leads to the following relations between the extrinsic (applied) voltages and the intrinsic voltages that actually control the channel.

$$V_{GS} = V_g + R_s I_d \tag{4}$$

$$V_{DS} = V_d + (R_s + R_d) I_d \tag{5}$$

R_s and R_d are comprised of the contact resistance and an access resistance associated with the rather large (2μm) spacing between the channel beneath the gate and the source and drain

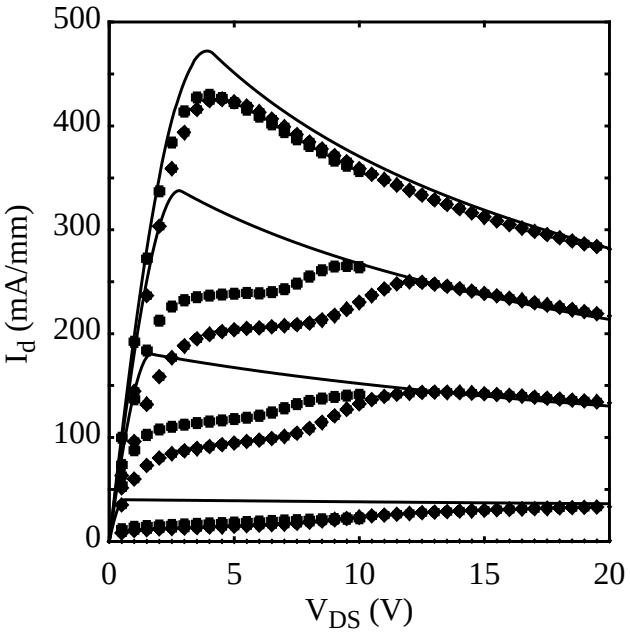

Figure 5: Comparison of the experimental (boxes 0 to 10V and diamonds 0 to 20V) and calculated (lines) drain current vs. drain-to-source bias in the absence of illumination. The gate voltages vary from 0 to -4V.

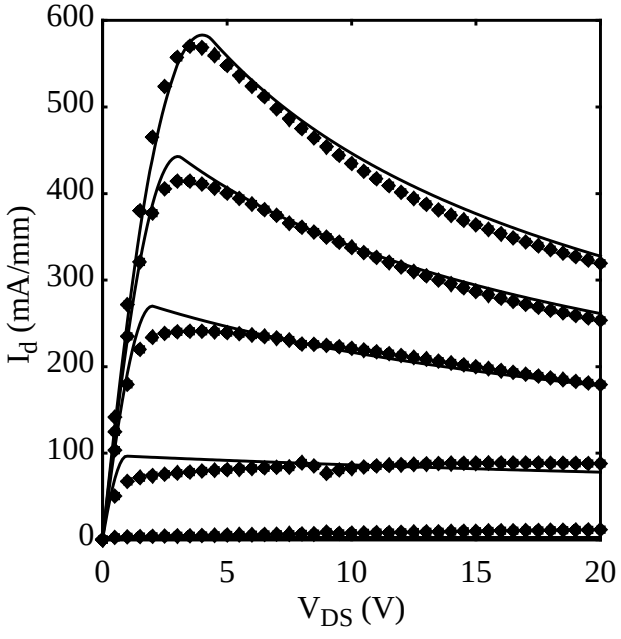

Figure 6: Comparison of the experimental (points) and calculated (lines) drain current vs. drain-to-source bias with device illumination. The gate voltages vary from 0 to -4V.

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contacts, both of which are determined by separate TLM measurements. Representative values for the sheet resistivity and specific contact resistance obtained for the wafer examined here are ρ = 550...790Ω/❑, depending on the location on the wafer, and R_c = 0.6Ω·mm. Series resistances may be reduced by lowering the contact resistance through improvements in the process and by lowering the access resistance through a reduction of the source-to-drain spacing. The former effect is clearly evident in Figure 4 where measured contact resistances for different alloying conditions are shown. The contact resistance can affect the current through a device as is shown in Figure 4. This data will be discussed in a forthcoming paper.

The second extrinsic effect is the self-heating of the device due to power dissipation. In order to obtain the ambient temperature of the channel which enters the electron velocity through eq. (3), the device temperature is determined from $T = T_0 + R_{th}I_dV_{DS}$. Here R_{th} is the thermal impedance and T_0 is the temperature of the heat sink at the backside of the substrate (T_0 = 300K). The specific thermal impedance of the device structure is determined independently by using a two-dimensional device simulator and is found to be well approximated by $24\cdot(1 + (T-T_0)\cdot10^{-3})$K·mm/W, where the temperature dependences of the thermal conductivities have been taken into account.

With its parameters determined either by independent calculations or direct measurements, the HFET model is run until self-consistent solutions for given V_{DS} and V_{GS} are reached.

RESULTS AND DISCUSSION

Figure 5 shows measured HFET output characteristics with the device in the dark. The data are taken sequentially, starting with V_{DS} sweeps from zero to V_{DSmax} for V_{GS} = 0, -1, -2, -3V. The calculated results are also displayed. All model parameters are consistent with TLM , C-V, and Hall data from this wafer. The thermal impedance is obtained from a separate simulation, as indicated above. Clearly the agreement between the data and the model results is quite good for large V_{DS}. In particular, the strong negative output conductance caused by the self-heating is well reproduced. For small and intermediate V_{DS} the model predicts larger currents than observed experimentally. We tentatively attribute the discrepancy to trapping of (primarily hot) electrons. Under high drain bias conditions the traps are either emptied or their electrostatic effect is reduced and the drain current approaches the model values.

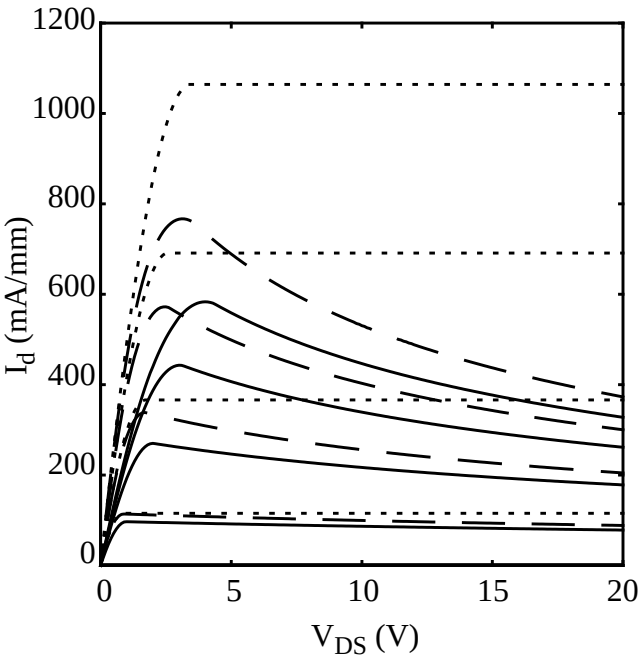

Figure 7: Comparison of expected HFET output characteristics of a device with decreased contact-to-channel spacing and reduced contact resistance (dashed curves) to the results of Figure 6 (solid curves). Also shown are the results expected for a perfectly heat sunk device (dotted curves).

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A more detailed analysis of the low voltage characteristics shown in Figure 5 will be the subject of future work. However, to substantiate the trapping hypothesis, the output characteristics of the same device under illumination by a Hg pen lamp are examined in Figure 6 and compared to the model results. Due to the illumination, traps are unlikely to be occupied by electrons, the sheet resistivity decreases, and the output currents increase, particularly at low voltages. The agreement between the model and the data over the full drain-to-source voltage range under these conditions is very good. The maximum ambient temperature of the channel region is found to be approximately 500K.

Lastly, the limitations imposed on the device performance by the series resistances and by the thermal effects are examined in Figure 7. Here, the model results of Figure 6 are compared to the performance that would be expected from the same transistor structure, but with a contact resistance of 0.1 Ω·mm, a value that is typical of AlGaAs/GaAs HFETs [9], and gate-to-source and gate-to-drain contact spacings of 0.5μm (dashed curves). Also shown is the additional consequence of ideal heat sinking that completely eliminates the thermal effects (dotted curves). Clearly, even an improvement in series resistance alone can lead to larger ouput currents. A very significant improvement is predicted if the self-heating of the device can be suppressed.

The present comparison of results from a self-consistent model that includes parasitic resistances and self-heating effects indicates that considerable improvement in the output current densities of AlGaN/GaN HFETs can be expected even for relatively long channel devices. The model accounts well for experimentally observed DC output characteristics without resorting to the introduction of arbitrary parameters.

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