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Added Information to TEM Samples by Chemical Stain – Applications to Silicon Devices

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Demand for TEM increases as device features shrink to nanometer geometry due to TEM high resolution and high contrast capability. Chemical staining methods have not routinely been practiced on TEM samples mainly due to the sample fragileness and thickness variation. With the use of a dicing saw [1] and a FIB, TEM samples are now much more controllable and sturdy for chemical staining. The objective of this presentation is to show 4 different stain solutions and methods to retrieve additional information that are difficult or not possible without stain.

1. Junction stain application for 2D junction profile*
The solution developed in TI is specifically for FIB prepared TEM samples. To remove the FIB damage layer, the sample was first dipped into a diluted HF with nitric acid solution prior to the junction etch. To increase the selectivity and to reduce the etch rate for better control, the junction etch solution is made of acetic buffered HF and nitric acid. DI water is used in between steps to stop etch. The solution has been routinely applied to various devices from 0.35 um to 60 nm technology nodes (figs. 1 – 4). (*TI-US patent pending)

2. Silicon stain for gate oxide imaging
The above solution can be used to partially etch the silicon but leave gate oxide intact on a TEM sample. With this treatment, it is possible to reveal ultra-thin gate oxide with clarity and across the whole gate length (figs. 5- 6).

3. Copper stain
A nitric solution was developed to etch out the copper in the copper interconnects to reveal details of the barrier coverage and plug sidewall texture which are not easily seen in normal TEM or STEM images (figs. 7- 8).

4. Tungsten stain
Tungsten used in the contacts or vias are hard to milled and usually ended thick in the TEM sample. With a hydrogen peroxide solution, the tungsten can be easily removed to reveal structure behind or under the tungsten (figs. 9-10).

The techniques shown here have been applied to delineate 2-D junction profile with sub-nanometer resolution for all technologies, to reveal ultra-thin gate oxide that is very difficult to obtain from FIB prepared TEM sample, to characterize contacts and via barrier integrity. In some cases, it helps pin point device failure mechanism.

References
[1] L. Tsung et al., M.A. O'Keefe, Proc. Microsc. Microanal. (2000) 500.

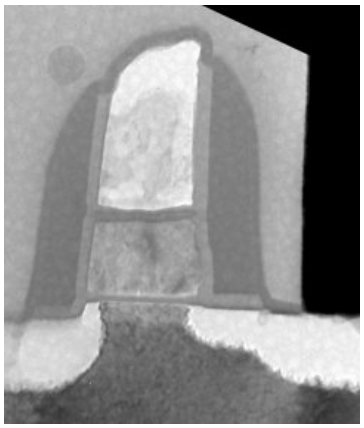


Fig. 1 – A flash cell

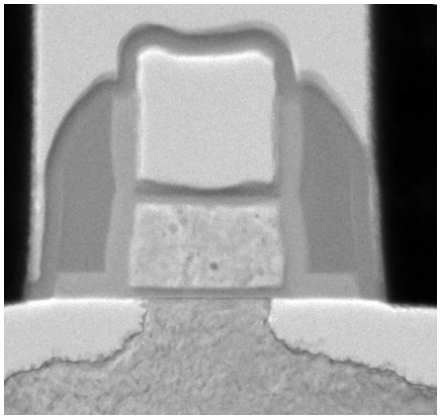


Fig. 2 – A flash cell

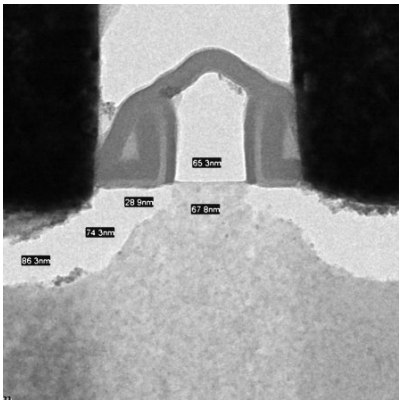


Fig. 3 – 90 nm transistor

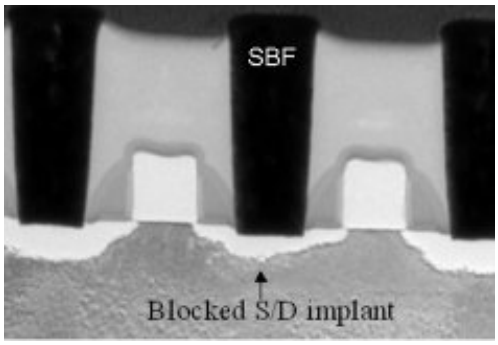
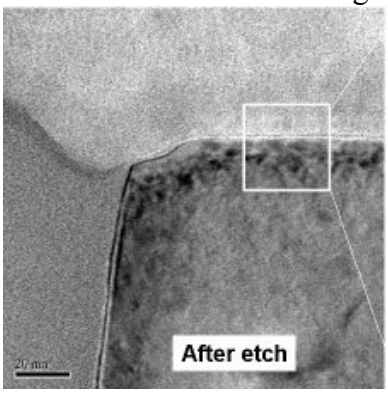
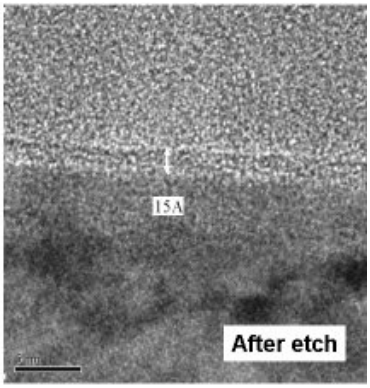
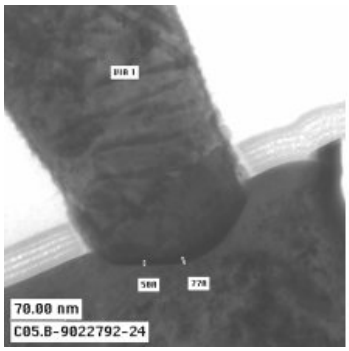


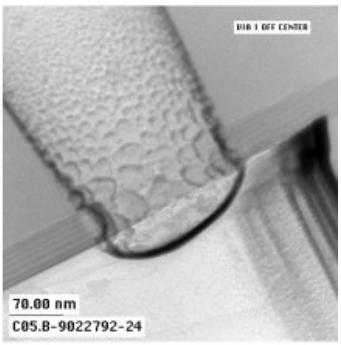
Fig. 4 - Junction stain for failure analysis



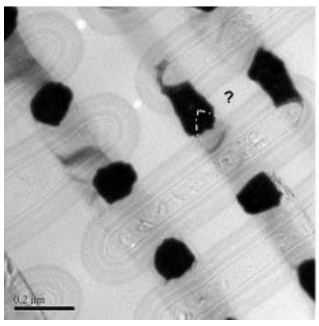


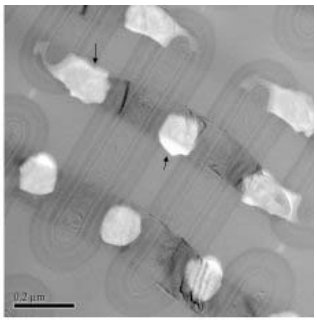
Figs. 5 & 6 - thin gate oxide after stain





Figs. 7 & 8- Cu via before and after stain





Figs. 9 & 10- W contacts before and after stain

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