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ATOMIC LAYER DEPOSITION FOR EMERGING THIN-FILM MATERIALS AND APPLICATIONS

FOCUS ISSUE

Multilevel memory and synaptic characteristics of a-IGZO thin-film transistor with atomic layer–deposited $Al_2O_3/ZnO/Al_2O_3$ stack layers

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A multilevel nonvolatile memory based on an amorphous indium–gallium–zinc oxide thin-film transistor is successfully demonstrated by using an atomic layer–deposited ZnO film as a charge trapping layer. The memory device shows a much higher erasing efficiency at a negative bias, i.e., after erasing at −13 V for 1 μs, the threshold voltage shift is as large as −7.4 V. In the case of 13 V/1 μs programming (P) and −12 V/1 μs erasing (E), the device demonstrates an ON/OFF readout drain current (I_{DS}) ratio of ∼10^3 after 10^5 s, and a large and stable ON/OFF I_{DS} ratio of ∼10^6 till 10^4 of P/E cycles. Furthermore, multilevel memory characteristics are also demonstrated on the device, showing an I_{DS} ratio of >10^2 for 4 different states. Additionally, the device also successfully demonstrates typical synaptic behaviors, such as excitatory and inhibitory postsynaptic current with different memory times at different memory states.

Introduction

Recently, amorphous indium–gallium–zinc–oxide (a-IGZO) thin-film transistor (TFT) nonvolatile memories have been widely researched as next-generation memory devices for flexible electronics and transparent panel systems [1, 2, 3, 4]. This is because a-IGZO has many advantages over conventional amorphous or polycrystalline silicon, such as high electron mobility, good uniformity, low processing temperature, and visible light transparency [5]. However, the a-IGZO TFT memory cannot be electrically erased by injecting holes into the charge storage layer from its channel, since a-IGZO is a natural n-type semiconductor and hole conduction is hard to generate under negative gate biasing [6, 7, 8]. Although light erasing [8, 9] or light-assisted electrical erasing [7] was reported to improve the erasing efficiency of the devices, electrical erasure with a high efficiency is eagerly desired for a-IGZO TFT memory from the viewpoint of practical application. Recently, some researchers reported that the a-IGZO TFT memories with an IGZO or ZnO charge trapping layer (CTL) exhibited electrically erasable characteristics [10, 11, 12]. However, most of them demonstrated an erasing bias as high as −20 V and a relatively long erasing time even up to 1 s [11, 12]. Moreover, it was also reported that the a-IGZO TFT memory with an a-IGZO CTL could be erased under a gate bias of 12 V and a high drain bias of 10 V, a threshold voltage shift (ΔV_{th}) of −3.88 V is obtained for an erasing duration of 10 ms [13]. All these practices will cause concerns about power consumption.

On the other hand, the demand for low-cost and high-density storage devices is pushing the physical scaling in charge trapping flash (CTF)-type memory devices. Thus, multilevel memory per cell is an urgent requirement in existing memory technology to increase the memory capacity without the need of stringent scaling. Furthermore, multi-functionalization of one device can improve circuit integration and reduce space occupation. In the past few years, synaptic devices that can emulate the signal transfer behaviors of the biological synapses have been paid more attention, which is ascribed to the necessity of the synaptic devices for building up the neuromorphic electronic systems [14, 15]. Therefore, it is meritorious to explore whether the a-IGZO TFT device can realize both memory and synaptic functions.

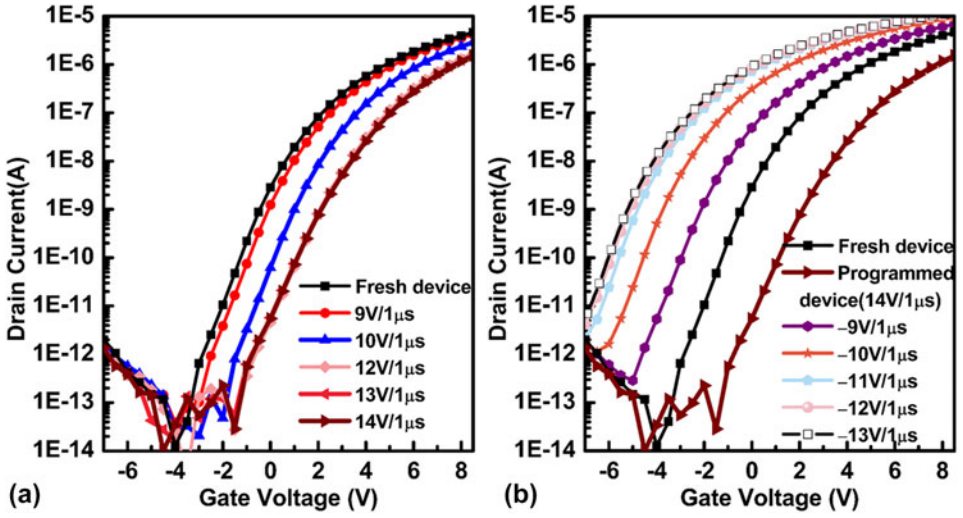

Figure 1: (a) The programming characteristics of the a-IGZO TFT memory device under various positive gate biases. (b) The erasing characteristics of the programmed device under various negative gate biases.

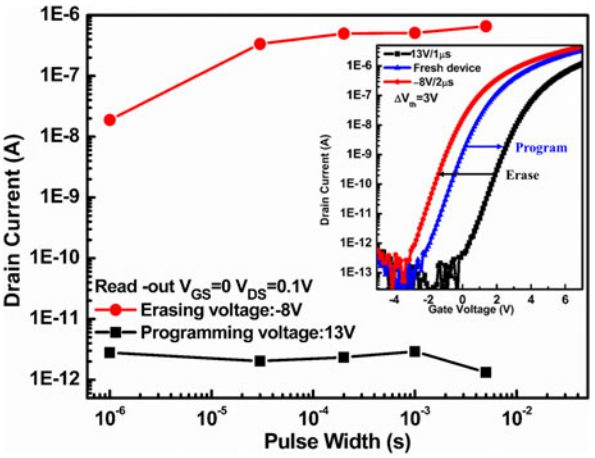

Figure 2: Variations of I_{DS} as a function of pulse width for the memory devices in ON and OFF states. The programming voltage corresponding to the OFF state was fixed at 13 V, and the erasing voltage corresponding to the ON state was kept at −8 V. The inset shows the successive programming and erasing characteristics of the device.

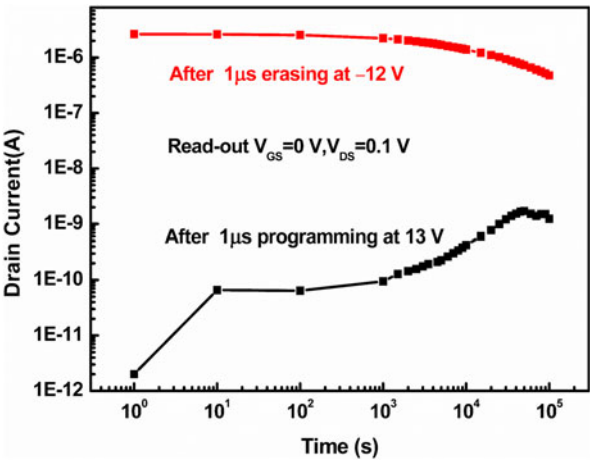

Figure 3: Dependence of I_{DS} on time for the memory devices in the ON and OFF states, which were obtained by applying −12 V/1 μs and 13 V/1 μs pulses to the gate, respectively. The I_{DS} was measured under V_{GS} = 0 V and V_{DS} = 0.1 V at room temperature.

In this article, a novel multilevel a-IGZO TFT memory cell is successfully demonstrated by using atomic layer–deposited $Al_2O_3/ZnO/Al_2O_3$ multilayers, where the ZnO layer acts as a CTL. In particular, the device exhibits a superior erasing efficiency under negative gate biasing. Moreover, the memory cell also demonstrates interesting synaptic behaviors.

Results and discussion

Figure 1 shows the programming and erasing characteristics of the a-IGZO TFT memory device under various gate biases. In terms of programming, the transfer curve moves gradually toward a positive bias as a function of programming voltage while keeping the programming time at 1 μs. The resulting ΔV_{th} relative to the fresh device increased from 0.3 to 2.3 V as the programming voltage increased from 9 to 13 V, followed by a programming saturation, as shown in Fig. 1(a). The number of electrons captured by the CTL was calculated to be 8.5 × $10^{22}/cm^2$ according to Eq. (1) [16]:

$$Q = C_{ci}\,\Delta V_{th} \quad , \qquad (1)$$

where Q is the stored electron density captured by the CTL, ΔV_{th} is the memory window, and C_{ci} is the gate dielectric capacitance per unit area. Such a significant ΔV_{th} suggests that considerable electrons from the n-type a-IGZO channel are injected into the ZnO CTL. Figure 1(b) shows the electrical erasing characteristics of the programmed device as a function of erasing voltage. As the erasing bias is enhanced from −9 to

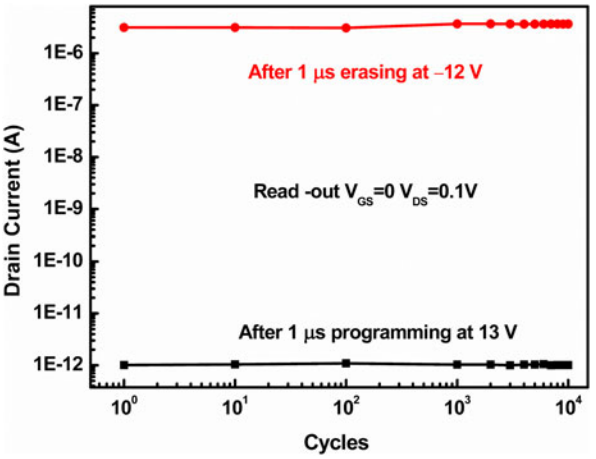

Figure 4: Variations of I_{DS} as a function of P/E cycles for the memory device. The P and E conditions correspond to 13 V/1 μs and −12 V/1 μs, respectively. The readout drain current (I_{DS}) was measured under V_{GS} = 0 V and V_{DS} = 0.1 V at room temperature.

TABLE I: Comparison of the ON/OFF of various a-IGZO TFT memories with different gate stacks.

Gate stack	Erasing conditions	ON/OFF I_{DS} ratio	Ref.
Al_2O_3/IGZO/Al_2O_3	−20 V/1 s	10^6	[10]
Al_2O_3/IGZO/Al_2O_3	−14 V/1 s	10^6	[17]
Al_2O_3/ZnO/Al_2O_3	−20 V/100 ms	10^7	[18]
Al_2O_3/ZnO/Al_2O_3	−20 V/1 s	10^8	[12]
SiO_2/ZnO/SiO_2	6 V/1 s	10^3	[19]
Al_2O_3/ZnO/Al_2O_3	−12 V/1 μs	10^6	Our work

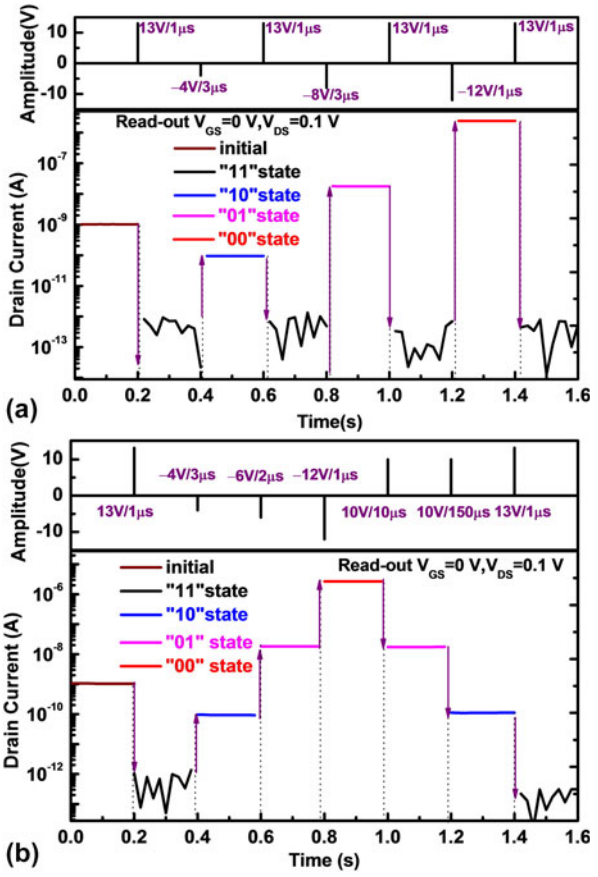

Figure 5: The multilevel memory performance of the devices: (a) mutual switching between "11" and "10", "11" and "01", and "11" and "00," respectively; (b) continuous switching from "11" → "10" → "01" → "00", and vice versa.

−13 V, the transfer curve shifts in the direction of a negative bias. After erasing at −13 V for 1 μs, a ΔV_{th} as large as −7.4 V is achieved. The number of positive charge captured by the CTL was calculated to be 2.7 × 10^{23}/cm^2. These results illustrate superior electrically erasable characteristics of the memory devices. Furthermore, an erasing saturation also appears when the erasing bias increases to −12 V.

Figure 2 shows dependence of the readout drain current (I_{DS}) of the memory on pulse width under programming and erasing modes. In terms of programming at 13 V, the programmed device exhibits a small I_{DS} (i.e., less than 1 × 10^{-11} A) when the gate bias is zero. This is because the trapped electrons in the CTL repel electrons in the channel, thus reducing the electron concentration in the channel. With respect to erasing at −8 V, the erased device shows a large I_{DS} (i.e., larger than 1 × 10^{-8} A) when the gate bias is zero. This should be attributed to the trapped positive charges in the CTL, which induces additional electrons in the channel, hence increasing the electron concentration in the channel. Therefore, the former is defined as an OFF state, corresponding to a programmed device, and the latter is defined as an ON state, corresponding to an erased device. Furthermore, as the pulse width increases from 1 × 10^{-6} to 5 × 10^{-3} s, the I_{DS} in the OFF state does not show an evident variation trend. However, the I_{DS} in the ON state demonstrates a gradual increase with the pulse width, i.e., I_{DS} rises from 2 × 10^{-8} to 6.5 × 10^{-7} A with increasing the pulse width from 1 × 10^{-6} to 5 × 10^{-3} s. That is, the ON/OFF I_{DS} ratio increases from ~10^4 to ~10^6, which means an increasing memory window as a function of pulse width. Furthermore, the inset in Fig. 2 indicates that the memory device can be easily switched between the programmed state and erased state, demonstrating a large memory window of 3 V after 13 V/1 μs programming and −8 V/2 μs erasing.

Figure 3 shows the memory retention characteristics by monitoring time-dependent I_{DS} in the ON and OFF states. In terms of 13 V/1 μs programming and −12 V/1 μs erasing, the ON/OFF I_{DS} ratio still remains ~10^3 after 10^5 s. Figure 4 shows the endurance characteristics of the memory as a function of P/E cycles. In the case of the above-mentioned P/E conditions, the device exhibits a stable and large memory window, i.e., the ON/OFF I_{DS} ratio is as large as ~10^6 till 10^4 of P/E cycles. Table I compares the erasing characteristics of various reported a-IGZO TFT memories and the current device. It is found that

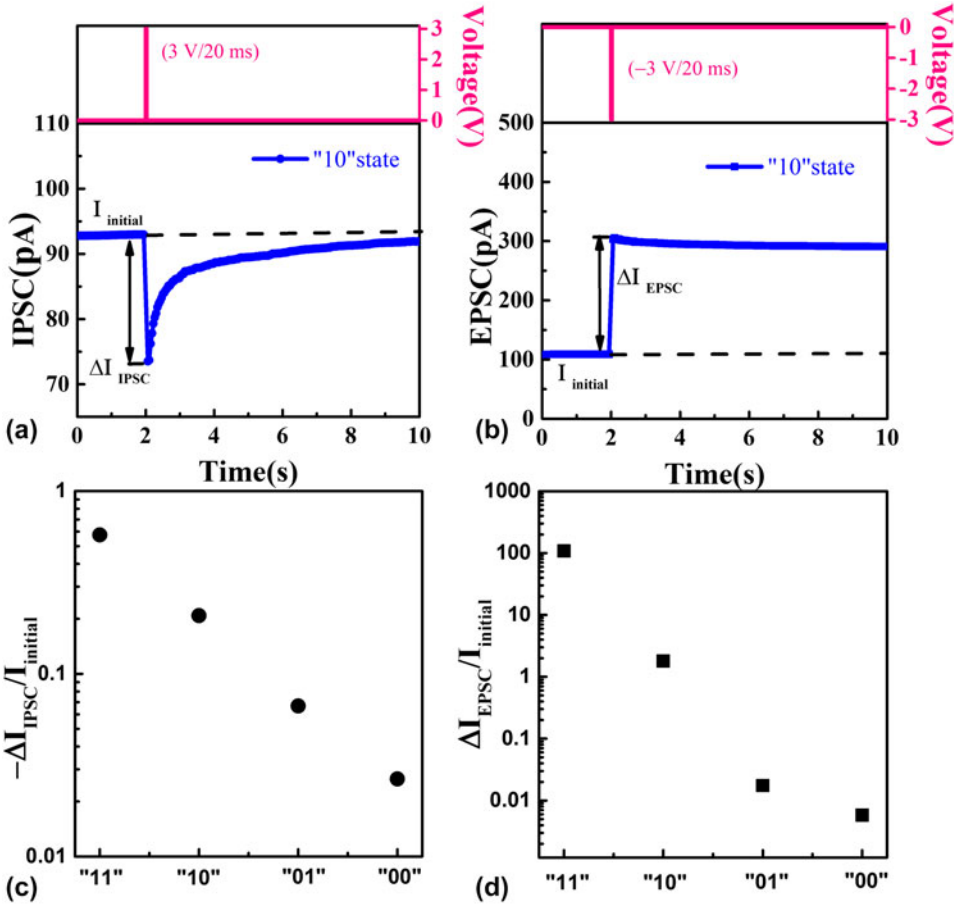

Figure 6: (a) Typical IPSC curve recorded from the memory device corresponding to "10" state in response to one positive presynaptic spike (3 V/20 ms); (b) typical EPSC curve recorded from the memory device corresponding to "10" state in response to one negative pre-synaptic spike (−3 V/20 ms); (c) normalized IPSC ($-\Delta I_{IPSC}/I_{initial}$) for different memory state; and (d) normalized EPSC ($\Delta I_{EPSC}/I_{initial}$) for different memory states.

our device exhibits a much higher erasing efficiency under a low bias (−12 V) and a short time (1 μs).

A multilevel memory cell is also demonstrated for the devices, as shown in Fig. 5(a). After programming at 13 V for 1 μs, the fresh device becomes the "11" state corresponding to an I_{DS} of $\sim 1 \times 10^{-12}$ A. Subsequently, the device is erased at −4 V for 3 μs and becomes the "10" state corresponding to an I_{DS} of $\sim 1 \times 10^{-10}$ A. When the erased device is reprogrammed at 13 V for 1 μs, it recovers to the "11" state again. If the erasing bias is enhanced to −8 V, the resulting I_{DS} increases to 2×10^{-8} A for 3 μs of erasing time, defined as "01" state. If the erasing bias is enhanced to −12 V, the I_{DS} increases to 2×10^{-6} A for 1 μs erasing time, labeled as the "00" state. Therefore, four states per cell with an enough large I_{DS} ratio ($\geq \sim 10^2$) between any two states are achieved by adjusting erasing conditions. Furthermore, continuous switching among these states is also illustrated in Fig. 5(b). The memory device can be switched from "11" → "10" → "01" → "00" state, and vice versa. For example, the "11" state is switched to the "10" state after erasing at −4 V for 3 μs. Following erasing at −6 V for 2 μs, the "10" state can be further switched to the "01" state. It is worth mentioning that the I_{DS} corresponding to different states can be modulated by well-engineering programming and erasing operations to achieve desired current levels to detect different electrical memory states.

Recently, synaptic devices have attracted much attention because of their potentials in neuromorphic electronic systems. Therefore, it is of significance to explore whether the a-IGZO TFT memory can be used for synaptic transistors, especially under different memory states. To investigate the synapse-emulating behaviors of the a-IGZO TFT memory, a presynaptic spike needs to be applied to the bottom gate of the device while the drain current of the device is measured as a function of time at some source-drain voltage (V_{ds}). Thus, the resulting drain current is defined as an inhibitory postsynaptic current (IPSC). Similarly, if a negative presynaptic spike (−3 V/20 ms) is applied to the back gate, the resulting drain current is defined as an excitatory postsynaptic current (EPSC). Figures 6(a) and 6(b) show the typical IPSC and EPSC of the memory device associated with "10" state in response to presynaptic spikes of 3

V/20 ms and −3 V/20 ms, respectively, at V_{ds} = 50 mV. In general, the interface traps between the a-IGZO channel and the Al_2O_3 gate dielectric can capture electrons under a positive presynaptic spike, and this leads to a decrease in the drain current. After removal of the spike, the captured electrons are gradually de-trapped, hence resulting in a gradual recovery of IPSC toward the initial drain current, as indicated in Fig. 6(a). Furthermore, it is reported that neutral oxygen vacancies in a-IGZO act as shallow donors, and under a negative gate bias, some neutral oxygen vacancies (V_O) in the a-IGZO channel become positively charged due to lowering of the Fermi level for electrons (E_F) at the surface of the a-IGZO channel [20]. Thus, the negative presynaptic spike can give rise to accumulation of positively charged oxygen vacancies at the a-IGZO/Al_2O_3 interface, thus increasing the drain current, as shown in Fig. 6(b). After the negative spike, the resulting EPSC exhibits very small attenuation. This could be attributed to low-speed departure of positively charged oxygen vacancies from the interface. In the current experiment, it is much interesting to find that both the IPSC and EPSC curves of the devices exhibit obvious difference for different memory states, as shown in Figs. 6(c) and 6(d). As the memory state changes from "11" → "10" → "01" → "00", both the normalized IPSC and EPSC decrease gradually. This should be related to the amount and type of charges trapped in the ZnO layer under different memory state, which further interact with the presynaptic spike, finally determining the electron concentration in the channel. In a word, the a-IGZO TFT memory successfully demonstrates the emulation of synaptic behaviors and exhibits tunable EPSC/IPSC properties along with various memory states.

Conclusion

The multilevel a-IGZO TFT memory cell is achieved by using atomic layer deposition (ALD) ZnO as a CTL. The device shows a much higher erasing efficiency at a negative bias, as compared with conventional a-IGZO TFT-based memories, which exhibited poor erasing characteristics. The device exhibits good endurance and promising retention characteristics. Additionally, typical synaptic behaviors including EPSC and IPSC with different memory times at different memory states were also successfully demonstrated.

Methods

A cleaned p-type Si(100) wafer (ρ = 0.001–0.005 Ω cm) was used as the starting substrate, which served as the back gate of the device. Then, multilayers of Al_2O_3 (35 nm)/ZnO (20 nm)/Al_2O_3 (8 nm) were successively deposited by ALD, which were used as the blocking layer, CTL, and tunneling layer, respectively. Herein, the precursors for ALD Al_2O_3 and ZnO films were $Al(CH_3)_3/H_2O$ and $Zn(C_2H_5)_2/H_2O$, respectively. After that, a 40 nm a-IGZO film was deposited by radio frequency magnetron sputtering at room temperature using an $InGaZnO_4$ target under the conditions, i.e., Ar = 50 sccm, power = 110 W, and working pressure = 0.87 Pa. Subsequently, the active channel was defined by photolithograph and wet etch, and then 30 nm Ti/70 nm Au bilayer electrodes were formed by e-beam evaporation and lift-off technique. Finally, the fabricated device was annealed at 250 °C in O_2 for 5 min.

Electrical measurements were performed on the devices with a channel length (L = 10 μm)/width (W = 60 μm) using a semiconductor device analyzer (Agilent B1500A) at room temperature.

Acknowledgments

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