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Recent Developments in Automated Sample Preparation for FESEM

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Analytical practice in the semiconductor industry requires rapid, efficient and reliable cross – sectional sample preparation prior to FESEM.[1] An integrated preparation technique has been developed that combines plasma cleaning (PC), argon ion beam etching (IBE), reactive ion beam etching (RIBE), reactive ion etching (RIE), and ion beam sputter coating (IBSC) in a single vacuum chamber, Fig. 1.[2] PC incorporates an inductively coupled, RF generated (Ar– 25%O_2) plasma to remove residual hydrocarbons by chemical reduction to $CO/CO_2/H_2O$. The removal of contamination enhances the quality of subsequent processes and in particular the application of conductive coatings.[3, 4] IBE or RIBE requires that a sample be tilted and rotated in relation to an incident ion beam. For this research, a hollow anode discharge (HAD) ion source was utilized. Incident ions remove surface material by a combination of momentum transfer (IBE) and / or chemical reactivity (RIBE). At low (< 15^o) angles of incidence to the surface, ions tend to level or "planarize" rather than etch. At higher angles (>15^o), the incident ions tend to raise topography or "decorate" microstructural features. RIE requires a plasma to be formed from individual or mixed gases of CF_4, CHF_3, Cl_2, and O2, yielding reactive fluorine, chlorine and oxygen ions. Plasma chemistries are often produced that are selective to one or more components (Si, SiO_2, Al) of a microelectronic material.[5] The plasma chemistry is adjustable by independent control of the gas flow rates and chamber pressure. The energy of ionization is supplied by a shaped electrode driven by a RF power supply. The sample is both electrically grounded to promote the flow of positively charged, reactive ions to its surface and rotated to effect the desired surface characteristics. IBSC requires "line of sight" IBE of targets (C, Cr, Pt, W) to transfer the materials to a sample surface. Tilt / rotation of a sample promotes the deposition of thin (< 2 nm), structurally amorphous and uniform coatings that are preferred for high resolution FESEM.

In the microelectronic industry, optimal analysis of devices depends on cross sectioning for FESEM without altering the microstructure. A combination of polymers, metals and ceramics on silicon presents a challenge to the analyst. Cleaving or sawing may cause physical damage, especially of the metals. Physical damage is removable by further mechanical preparation, but residual smearing masks finely spaced porosity and interlayers. Use of abrasives, lubricants and embedding compounds may contaminate the material with organic compounds. For this research, mechanically ground (0.05 μm finish), cross sections of Pentium III materials were subjected to the series of previously mentioned treatments. The various operations were automatically sequenced within a single vacuum chamber. The processes were programmed and controlled by computer, including the duration of each treatment. An important step was the compensation for sample height at each processing position in the instrument. After optically sensing the sample height, the sample stage automatically positioned the sample surface in the appropriate plane(s) for each subsequent processing step.

Following mechanical grinding, the Pentium III microstructure exhibited gross damage, Fig. 2 (left). PC was performed first to remove any organic residues, followed by planarization using IBE (HAD: 4 kV, 5 mA, tilt angle = 10^o, 360^o rotation). RIE (Parallel Plate: 10W) with CF_4 – 10%O_2 was used to decorate the surface by selective removal of Si, and to a lesser extent, SiO_2. Samples were plasma cleaned for a second time, then examined with FESEM. Microstructural features within the metal lines, dielectric, interconnects ("plugs") and oxides were revealed. Pores within and bond lines separating the SiO_2 layers were exposed, Fig. 2 (right). Porosity within the W /Ti plugs was also evident. Since no significant charging occurred during low voltage imaging, conductive coatings were not applied in this case.

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References
[1] J. Petrus et al., The SEM Lab, From Logistics to Final Sample Preparation Techniques for SEM Analysis of Semiconductors, IBM Microelectronics, Hopewell Junction, New York, 2002.
[2] P.E. Fischione et al., Method and Apparatus for Preparing Specimens for Scanning Electron Microscopy, U.S. Patent Application.
[3] T. C. Isabell et al., "Plasma Cleaning and Its Applications for Electron Microscopy", Microsc. Microanal., 5 (1999) 126-135.
[4] J.I. Goldstein et al., Scanning Electron Microscopy and X-ray Microanalysis, Plenum, New York, 1981, pp. 461 – 494.
[5] S.M. Rossnagel, Handbook of Plasma Processing, Noyes Publications, New York, 1990, p. 207.

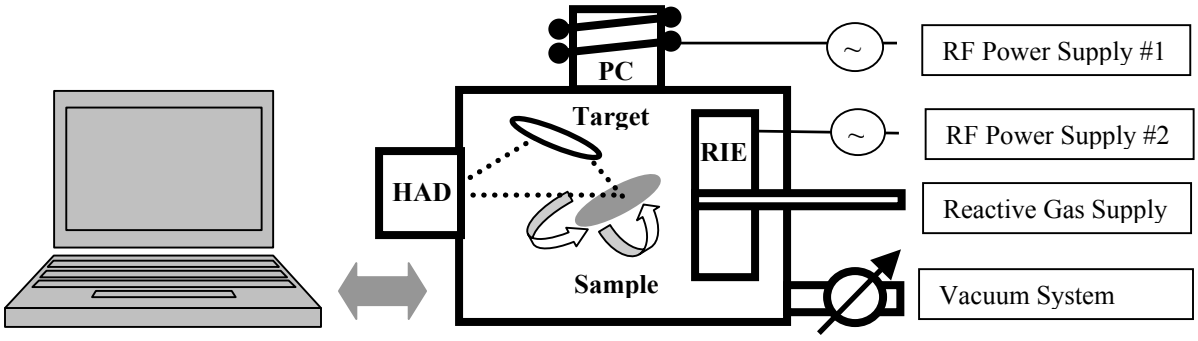

FIG. 1 Schematic of vacuum sample chamber.

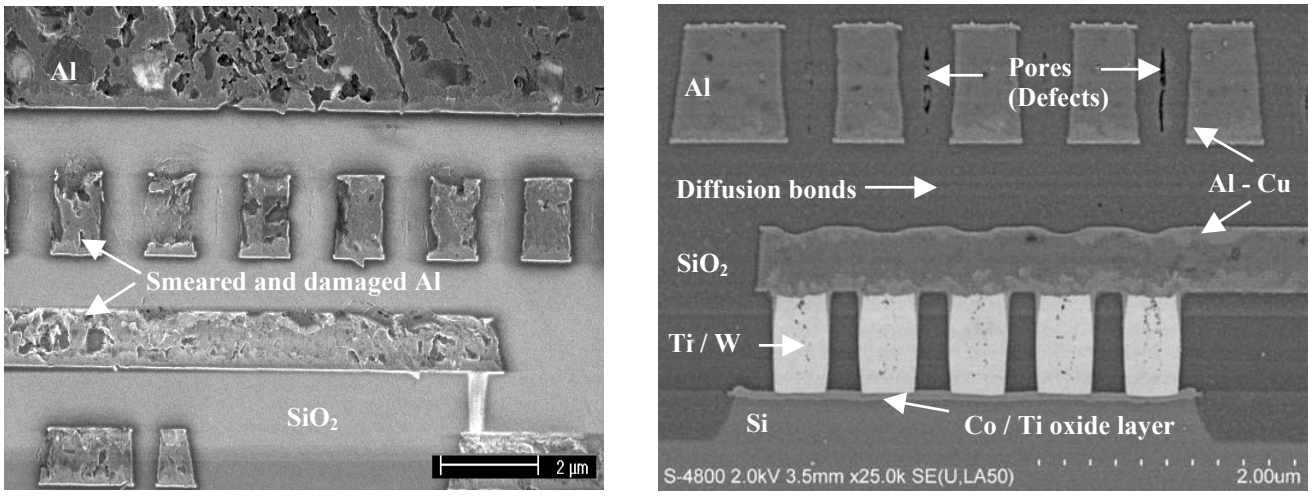

FIG 2: Microstructural features of Pentium III material before (left) and following (right) typical sample preparation by PC + IBE + RIE + PC

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