FABRICATION AND CHARACTERIZATION OF METAL-FERROELECTRIC-GAN STRUCTURES

W.P.Li, R.Zhang, J.Yin, X.H.Liu, Y.G.Zhou, B.Shen, P.Chen, Z.Z. Chen, Y.Shi, R.L.Jiang, Z.G.Liu, Y.D.Zheng
National Laboratory of Solid State Microstructure and Department of Physics, Nanjing University, Nanjing 210093, China
Z.C.Huang
Raytheon ITSS, 4500 Forbes Boulevard, Maryland 20771

ABSTRACT

GaN-based metal-ferroelectric-semiconductor (MFS) structure has been fabricated by using ferroelectric $Pb(Zr_{0.53}Ti_{0.47})O_3$ (PZT) instead of conventional oxides as gate insulators. The GaN and PZT films in the MFS structures have been characterized by various methods such as photoluminescence (PL), wide-angle X-ray diffraction (XRD) and high-resolution X-ray diffraction (HRXRD). The Electric properties of GaN MFS structure with different oxide thickness have been characterized by high-frequency C-V measurement. When the PZT films are as thick as 1 μm, the GaN active layers can approach inversion under the bias of 15V, which can not be observed in the traditional GaN MOS structures. When the PZT films are about 100 nm, the MFS structures can approach inversion just under 5V. All the marked improvements of C-V behaviors in GaN MFS structures are mainly attributed to the high dielectric constant and large polarization of the ferroelectric gate oxide.

I. INTRODUCTION

Recently, the semiconductor gallium nitride (GaN) has been recognized for several decades for their potential and, recently, commercial viability in wide band optoelectronic device applications [1]. The electronic devices that can be used for high power and high temperature applications have also been fabricated, among which GaN-based MOSFETs are actively studied [2]. The traditional GaN MOS structures fabricated with conventional oxides, like SiO_2 [3,4], Si_3N_4 [3], $Ga_2O_3(Gd_2O_3)$ [4], as insulators have to be improved. One important reason is that large applied voltage, which is incompatible with most other electronic devices, is imposed on all the previous GaN MOS structures. In our work, ferroelectric oxides have been used in GaN MOS structures to address this problem because of large polarization provided by ferroelectric and the high dielectric constant of ferroelectric gate.

Since the field-effect transistors (MFSFETs) was first proposed by Wu [5, 6], it has been extensively studied because of their applications in non-volatility and high speed memories and integration circuits [7-10]. Nowadays, the semiconductor used in metal-ferroelectric-semiconductor (MFS) structures usually is Si. The instability of the ferroelectric/Si interface due to interdiffusion between ferroelectrics and Si substrates has still impeded the development of the novel device [8]. Consequently, many kinds of buffer layers have been deposited between ferroelectrics and Si substrates to prevent the behavior of interdiffusion [11-13], which also decreases the control of ferroelectric polarization on the potential of Si surface. GaN is so stable that it can work without weight loss at 1000 ^{0}C[14]. GaN MFS structure is a good candidate to develop ferroelectric/semiconductor interface and MFSFETs with high-temperature stability.

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II. EXPERIMENTS

In the GaN MFS structure developed in this work, n-type GaN active layer is grown by light radiant heating low-pressure metalorganic chemical vapor deposition (LRH-LP-MOCVD) on the (0001) oriented sapphire (Al_2O_3) substrate which is pre-cleaned by organic solvents and H_2SO_4 : H_3PO_3(3:1) solutions [15,16]. Before the epitaxial growth of GaN layer, a thin GaN buffer (about 30nm) was deposited at 520 ^{0}C on sapphire substrate. Then the GaN active layer (n~10^{17}cm^{-3}) was deposited at 1040 ^{0}C. Afterwards, the ferroelectric $Pb(Zr_{0.53}Ti_{0.47})O_3$ (PZT) films with different thickness have been deposited directly on GaN films by pulsed laser deposition (PLD). The experimental condition is showed in the Table 1.

After the deposition of PZT, the samples are annealed in-situ in the chamber with 0.5 atm. O_2 for 30 minutes. In the following process, very thin SiO_2 films are deposited on thin PZT films (about 130 nm) by plasma enhanced chemical vapor deposition (PECVD) to decrease the leakage current. Then the top electrodes (about 200 nm) are fabricated by magnetron sputtering and patterned with a shadow mask of holes 0.2mm in diameter, while the bottom electrodes are contacted with aluminum (Al) from the edge of GaN top surface. Finally, the whole samples are annealed at the temperature of 600 ^{0}C after which excellent ohmic contacts on GaN are formed.

Table I. The experimental condition in the deposition of PZT by pulsed laser deposition (PLD)

Item	**Condition**
Target	ZrO_2, TiO_2 and PbO
Substrate	n-type GaN(0001)
Substrate temperature	750 ^{0}C
Deposition time	5~25 minutes
Laser wavelength	248 nm (KrF excimer)
Laser frequency	5 Hz
Laser power	2.5J/cm^2
ambient	O_2 (20 Pa)

III. DISCUSSION

The GaN films deposited by LRH-LP-MOCVD have been characterized by photoluminescence (PL) and high-resolution x-ray diffraction (HRXRD) methods. In the PL spectra, strong band-edge luminescence has been observed and undesirable YL peaks do not exist. The full width at half maximum (FWHM) of GaN in the HRXRD pattern is 8.6 min.

The PZT films directly on GaN (0001) are characterized by X-ray diffraction (XRD). The results show that the PZT films are deposited along the orientations of <100>, <110>, <211>

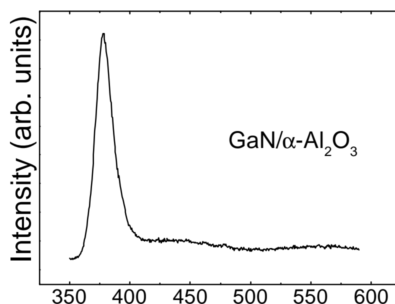

Figure 1 A typical PL spectrum of GaN on sapphire by LRH-LP-MOCVD.

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and <111>, among which the <110> peak is the strongest. No undesirable peak of pyrochlore phase appears in the XRD pattern, which shows that PZT films are well crystallized with perovskite structure.

The high-frequency capacitance-voltage (C-V) measurement is an important characterization method of MOS structures. When the applied bias are large enough to make the GaN surface approach depletion, the bias voltage (V_b) has been distributed between gate insulator (V_i) and depletion layer (V_d):

$$V_b = V_i + V_d \qquad (1)$$

The GaN MOS structures under the bias can be expressed as the two capacitors, the insulator capacitor (C_i) and depletion capacitor (C_d), in series. The voltage and capacitance distributions have the following relationship:

$$\frac{V_d}{V_i} = \frac{C_i}{C_d} \qquad (2)$$

Therefore, the bias voltage can be expressed into the following form:

$$V_b = (1 + C_d/C_i)V_d \qquad (3)$$

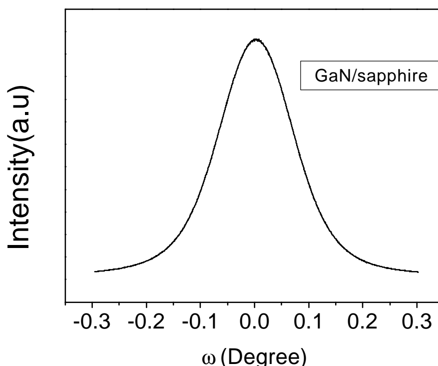

Figure 2 A typical HRXRD spectrum GaN on sapphire grown by LRH-LP-MOCVD.

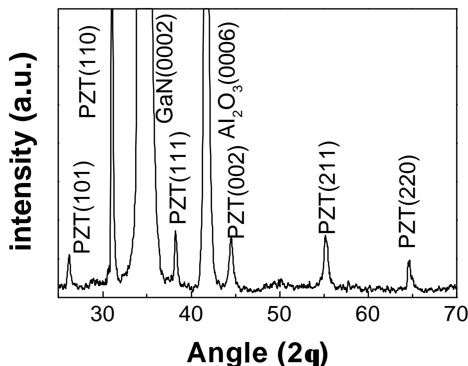

Figure 3. An X-ray spectrum of PZT directly on GaN (0001) by pulsed laser deposition.

As to a specific semiconductor sample, the V_d is a constant. Therefore, in order to decrease the bias voltage (V_b), we have to increase the insulator capacitance (C_i). In traditional GaN MOS structures with SiO_2 or Si_3N_4 as gate oxides, the effort made to decrease the large applied bias has focused on reducing the thickness of gate oxides, which results in the increase of C_d. However, these approaches to decrease the bias voltage are not desirable. It is very difficult to allow GaN to approach inversion under bias of 15 volts although the oxide insulators are thinner than 60nm [4].

In GaN MFS structures, the insulator capacitance (C_i) has been greatly increased because of the high dielectric constant of ferroelectrics. By using the ferroelectric oxides as gate insulators, we need not reduce the oxide thickness to increase the capacitance.

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Moreover, in the MFS structures, there are polarization fields (on the order of 10^6 V/cm) much larger than external applied field (on the order of 10^{-4}~10^{-5} V/cm) at the ferroelectric/semiconductor interfaces. Figure 4 shows the C-V behavior of the GaN MFS structures with 1 μ PZT films. We can find that the GaN MFS structures with thick gate oxides can approach inversion under the bias of 15 volts.

The GaN MFS structures with 100 nm PZT films have also been characterized by high-frequency C-V method. In Figure 5, we can find the applied bias has been decreased sharply. The GaN active layer can approach inversion just under 5V, which can satisfy the practical need of the GaN MOS structures.

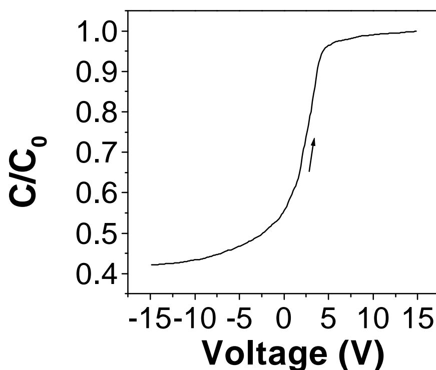

Figure 4 The C-V behaviors of GaN MFS structures with the 1 μ PZT films. The structures can approach reversion under 15 V, which is better than the C-V behaviors of GaN MOS structures with the same thick SiO_2 films.

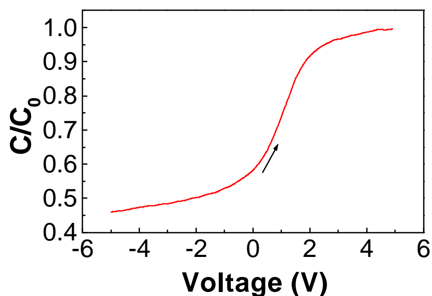

Figure 5 The C-V behaviors of GaN MFS structures with the 100nm PZT films. The structures can approach inversion just under small bias.

IV. CONCLUSION

In our work, GaN-based metal-ferroelectric-semiconductor (MFS) structures have been fabricated by using the ferroelectric oxide $Pb(Zr_{0.53}Ti_{0.47})O_3$ as gate insulators. The electrical properties of GaN MFS structures with different oxide thickness have been studied by the high-frequency C-V measurement. Due to the high dielectric constant and large polarization field of PZT films, the large applied voltage on conventional GaN MIS structures has been decreased sharply with comparison to that of traditional GaN MOS structures.

REFERENCES

1. T. Egawa, T. Jimbo, and M. Umeno, J. Appl. Phys. **82**,5816 (1997).
2. F. Ren, M. Hong, S. N. G. Chu, M. A. Marcus, M. J. Schurman, A. Baca. Appl. Phys. Lett. **73**. 3893. (1998).

https://doi.org/10.1557/S1092578300004816 Published online by Cambridge University Press

3. S. Arulkmaran, T. Jimbo, H. Ishikawa, S. Arulkumaran, T. Egawa. Appl. Phys. Lett. **73**. 809. (1998)
4. H. C. Casey. Jr., G. Gfoutain, R. G. Alley, B. P. Keller, and Steven P.DenBarrs. Appl. Phys. Lett. **68**. 1850. (1996).
5. S. Y. Wu, IEEE Trans. Electron Dev. **ED-21,** 499 (1973).
6. S. Y. Wu, Ferroelectrics **11,** 379 (1976).
7. Timonthy A. Rost, He Lin, and Thomas A. Rabson Appl. Phys. Lett. **59**, 3654(1991).
8. Marin Alexe. Appl. Phys. Lett. **72**, 2283. (1998)
9. Junji Senzaki, Koji Kurihara, Naoki Namura, Osamu Mitsunaga, Yoshitaka Iwasaki and Tomo Ueno. Jpn. J. Appl. Phys. **37**, 5150. (1998)
10. Takeshi Kijima and Hironori Matsunaga, Jpn. J. Appl. Phys. **37** (1998) 5171.
11. Junji Senzaki, Koji Kurihara, Naoki Nomura, Osamu Mitsunaga, Yoshitaka Iwasaki and Tomo Ueno, Jpn. J. Appl. Phys. **37** (1998) 5171.
12. Takeshi Kijika, Sakiko Satoh, Hironori Matsunaga and Masatoshi Koba, Jpn. J. Appl. Phys. **35** (1995) 1246.
13. Joon Lee, Young-Chul Choi, and Byung Lee, Jpn. J. Appl. Phys. **36** (1997) 3644
14. Y. Morimoto. J. Electrochem. Soc. **121**, 1381. (1974)
15. B. Shen, Y. G. Zhou, P. Chen, Z. Z. Chen, L. Zang, R. Zhang, Y. Shi. Y. D. Zheng. Appl. Phys. A **68**, 593. (1999)
16. Y. G. Zhou, B. Shen, Z. Z. Chen, P. Chen, R. Zhang, Y. Shi, Y. D. Zheng. Chinese Journal of Semiconductor **20**, 147. (1999)

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