Scanning Impedance Microscopy: From Impedance Spectra to Impedance Images

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The properties and performance of electronic devices are crucially dependent on interface-related phenomena. The presence of interfaces can enable electronic device functionality (*p-n* diodes, solar cells); alternatively, non-functional interfaces can degrade device performance (ohmic vs. non-ohmic contacts). The most versatile tools for semiconductor interface characterization are ac (impedance spectroscopy, *C-V*) and dc (*I-V*) transport measurements. However, due to the lack of spatial resolution, these methods often cannot separate the contributions from electroactive interfaces and contacts. This is especially true for the non-traditional electronic materials such as semiconductive oxides, nitrides, conductive polymers, etc. Combined with the tendency towards miniaturization of electronic devices, this clearly necessitates spatially resolved ac and dc transport measurements.

While dc transport properties have been shown to be accessible by measuring quasistatic surface potentials in laterally dc biased samples using both AFM and STM based potentiometric techniques,[1,2,3,4,5] until recently there was no technique for imaging of ac transport behavior. Scanning Impedance Microscopy is a novel scanning probe technique yielding impedance images of complex systems that can be easily correlated with traditional atomic force microscopy (AFM) images or other microscopies (TEM, SEM, optical). The experimental setup for SIM is similar to potential measurements under lateral bias and includes a cross-sectioned device connected in series with two current limiting resistors. Scanning Impedance Microscopy (SIM)[6] differs from other probe microscopies in that a modulating electric signal $V_{lat} = V_{dc}+V_{ac}\cos(\omega t)$ is applied laterally across the surface while the tip is held at constant bias V_{tip}. The surface topography is accounted for using the usual dual-pass scheme. The lateral bias induces oscillations in surface potential $V_{surf} = V_s + V_{ac}(x)\cos(\omega t + \varphi(x))$, where $\varphi(x)$ and $V_{ac}(x)$ are the position dependent phase shift and voltage amplitude and V_s is the dc surface potential. Oscillation in surface potential results in a periodic force acting on the dc biased tip. A lock-in system detects the phase, φ, and amplitude, A, of tip vibration, as shown in Figure 1. The local phase and amplitude of the cantilever oscillation constitute SIM phase and amplitude images at a given frequency. Under some very general assumptions, the phase lag between the surface voltage and cantilever oscillation is constant; therefore, by measuring the phase of the mechanical oscillations of the cantilever the position dependent phase, $\varphi(x)$ is obtained. The relationship between cantilever oscillation amplitude and voltage oscillation amplitude is less straightforward, but can also be explicitly obtained and $V_{ac}(x)$ can be mapped directly. Images can be acquired as a function of frequency from 300 Hz to ~100 kHz depending on the limitations of lock-in.

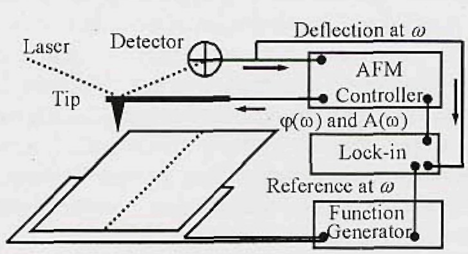

Figure 1: Experimental setup for scanning impedance microscopy.

In SIM the tip-cantilever system serves as a mechanical ac voltage sensor. This approach resembles 4 point resistivity measurements and impedance spectroscopy, but instead of two fixed voltage contacts a single potential probe is scanned across the surface obtaining the advantage of spatial resolution. In such a scheme the input impedance of the sensor is essentially infinite precluding a voltage divider effect.

For systems with a single electroactive interface (grain boundary, *p-n* junction, etc), an analytical expression for the phase shift across the interface, $\varphi_d = \varphi_1 - \varphi_2$, and the amplitude ratio, $\beta = A_2 / A_1$ (Figure 2), can be obtained as a function of interface capacitance, C_d, interface resistance, R_d, and resistance of circuit termination, R.[7]

In the low frequency limit, the SIM amplitude image visualizes <u>resistive</u> barriers at the interfaces. In the high frequency limit, voltage phase shift is determined by interface capacitance and circuit termination only, $\tan(\varphi_d) = 1/\omega C_d R$. In this limit, the SIM phase image directly visualizes <u>capacitive</u> interface barriers. For a resistively matched circuit, R R_d, the crossover correspond to frequencies ~ $1/C_d R_d$. Measuring frequency dependent amplitude ratio and phase shift in SIM allows interface resistance and capacitance to be determined quantitatively. Variation of dc potential bias across the interface allows local *C-V* and *I-V* properties to be obtained, as well.

The validity of this approach was verified against a known calibration standard - a cross-sectioned Schottky metal-semiconductor diode. Such standards are easily prepared and provide well-defined test structures for various electrostatic SPM techniques. SIM phase and amplitude images were acquired in the frequency range from 3 to 100 kHz. Figure 3(a) shows the phase profiles across the interface of a cross-sectioned device. Under forward bias condition no phase change occurs at the interface, while under reverse bias condition the depletion layer capacitance yields large phase shifts. The phase to the left and right of the interface in the reverse bias regime for two different circuit terminations is shown in Figure 3(b). The measured phase is the convolution of tip dynamics (harmonic oscillator; rapid change by 180° at the resonant frequency of the cantilever = 72 kHz) and lateral surface transport. Note that $\tan(\Phi_d)$ is linear in log-log coordinates with a slope of –1 corresponding to the high frequency

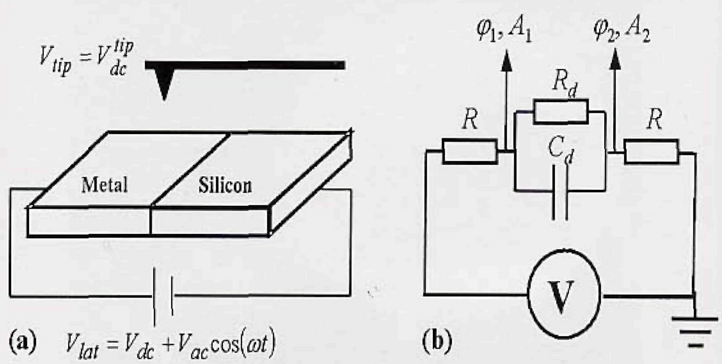

Figure 2: Schematic diagram of scanning impedance microscopy (a) and the equivalent circuit for SIM of a single interface (b). R_d and C_d are the (unknown) capacitance and resistance of the interface, R is the circuit termination resistors used in experimental setup. φ_1, φ_2, A_1 and A_2 are the measured phase and amplitude of mechanical cantilever oscillations on the left and right of the interface, from which interface properties can be determined.

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regime (Figure 3c). The interface capacitance can be calculated from the intercept and is shown in Table I.

The interface capacitance increases for large current limiting resistors *R*. This is due to the fact that for large *R* the potential drop at the interface is smaller; therefore, the width of the depletion region is also smaller and interface capacitance is higher. Thus, by varying the lateral dc bias during SIM imaging the *C-V* properties of the interface can be obtained as shown in Figure 4. Local potential drop at the interface, V_d, is determined as a function of lateral bias, V_{dc}, by Scanning Surface Potential Microscopy (SSPM), as shown in Figure 4 a. Phase vs. lateral bias curves differ by more than two orders of magnitude, depending on the circuit termination as shown in Figure 4 b. Capacitance calculated from phase and plotted as a function of potential drop at the interface forms a universal linear dependence (Figure 4 c). From the *C-V* dependence the Schottky barrier height is estimated as 0.6 ± 0.1 eV, as compared to 0.55 eV from conventional *I-V* measurements. This verifies that SIM yields quantitative information on interface capacitance. So it can be applied to other systems with single interfaces such as grain boundaries in semiconducting $SrTiO_3$ bicrystals. Figure 5 shows SIM phase and amplitude images across the grain boundary under different dc bias conditions. In the high frequency limit both *I-V* and *C-V* characteristics of the interface can be reconstructed from the SIM data.

Scanning Impedance Microscopy can be extended to the characterization complex materials. Figure 6 compares the surface topography, SIM phase at two different frequencies and SIM amplitude images of polycrystalline $BiFeO_3$. Phase changes at the interfaces clearly delineate *capacitive* barriers at the grain boundaries. The frequency dependence of interface phase shift across individual grain boundaries from SIM measurements can be compared with those calculated from macroscopic impedance spectra and perfect agreement was found. The amplitude doesn't change abruptly at the interfaces; rather it exhibits a uniform decrease throughout the sample, indicating ohmic losses within the grains.

SIM can be used to image interface behavior in more complex systems including ZnO varistors, grain boundaries in *p*-doped +Si (solar cell), Zener diodes, etc.[8] In some cases the observed SIM phase and amplitude images cannot be explained by simple *RC* interface approximations, suggesting that SIM accesses fundamental phenomena such as minority carrier generation at the grain boundaries. Lateral resolution in the direction normal to the interface is ~50 nm for the currently used experimental set-up. Certain electrostatic force sensitive scanning probe techniques (EFM) have been shown to provide electrostatic data with atomic

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R, kOhm	*Intercept*	*Slope*	C_d, 10^{-10} F	V_d, *V for* V_{dc} = -5 *V*
10	4.94 ± 0.02	-0.99 ± 0.01	1.83	4.83
47	4.21 ± 0.01	-0.98 ± 0.01	2.11	3.85
100	3.84 ± 0.01	-0.98 ± 0.01	2.32	2.86
220	3.29 ± 0.04	-0.98 ± 0.02	3.76	0.80

Table I: Frequency dependence of SIM phase shift

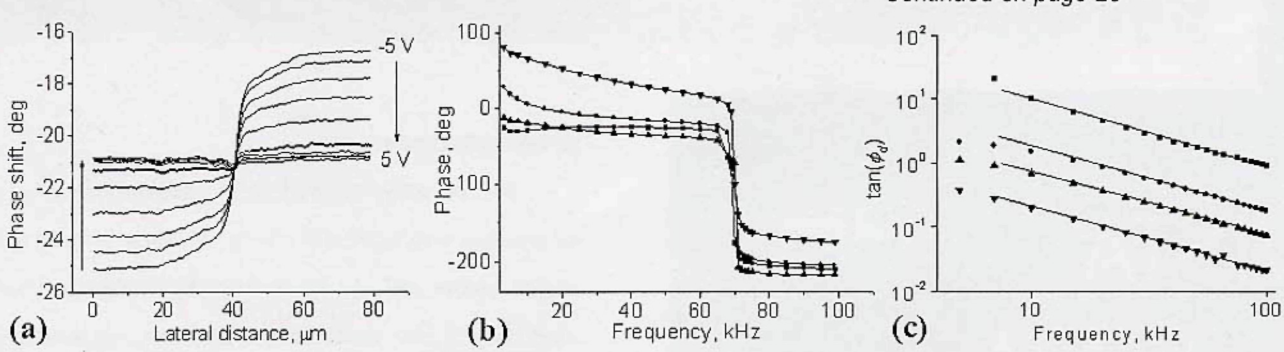

Figure 3: Phase profiles across a metal-semiconductor interface as a function of lateral dc voltage (a), frequency dependence of SIM phase on the left and right of the interface for *R* = 10 kOhm (▲, ▼) and 100 kOhm (■, ●) (b) and frequency dependence of phase shift of the interface for circuit terminations 10 kOhm (■), 47 kOhm (●), 100 kOhm (▲) and 220 kOhm (c).

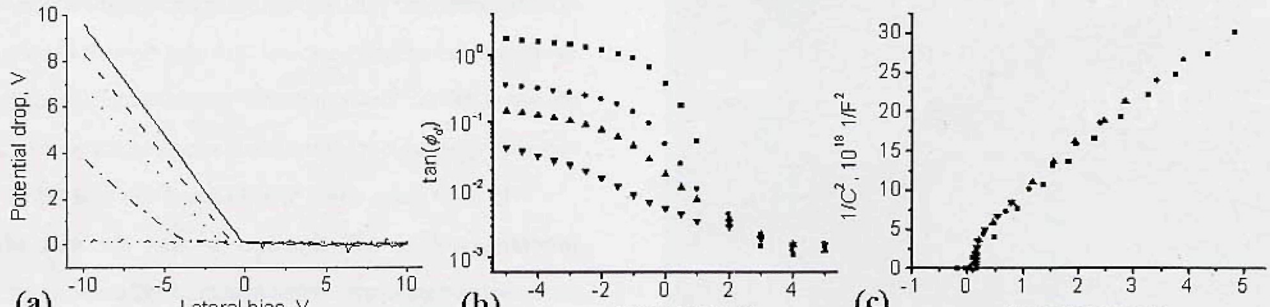

Figure 4: Potential drop at the interface as a function of external bias for circuit terminations 10 kOhm (——), 47 kOhm (- - - - -), 100 kOhm ( ), 220 kOhm (— - —), and 1 Mohm (— - - —) (a), SIM phase angle shift at 50kHz vs. lateral dc bias (b) and interface capacitance vs. potential drop at the interface © for circuit terminations 10 kOhm (■), 47 kOhm (●), 100 kOhm (▲), and 220 kOhm (▼)

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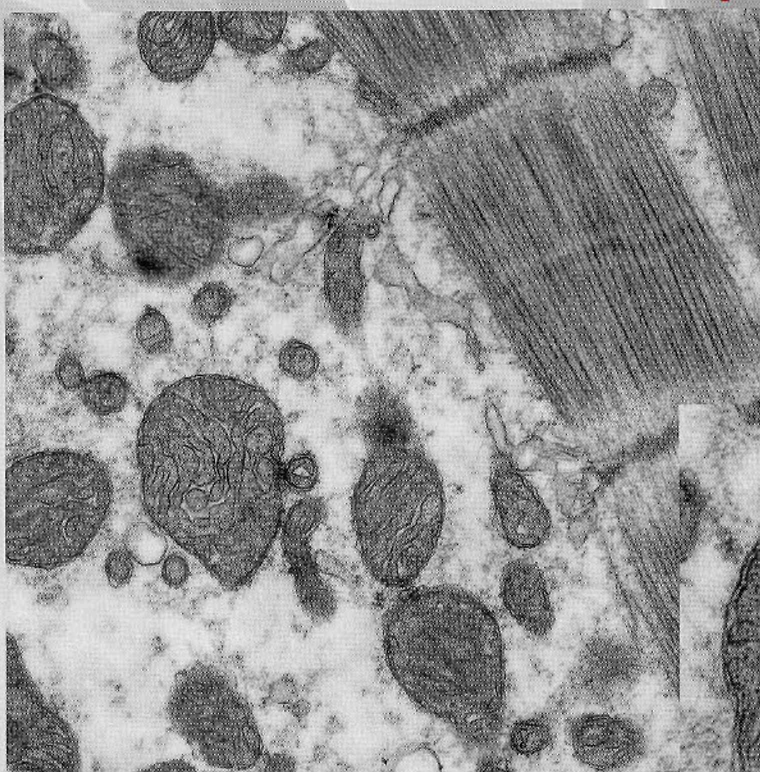

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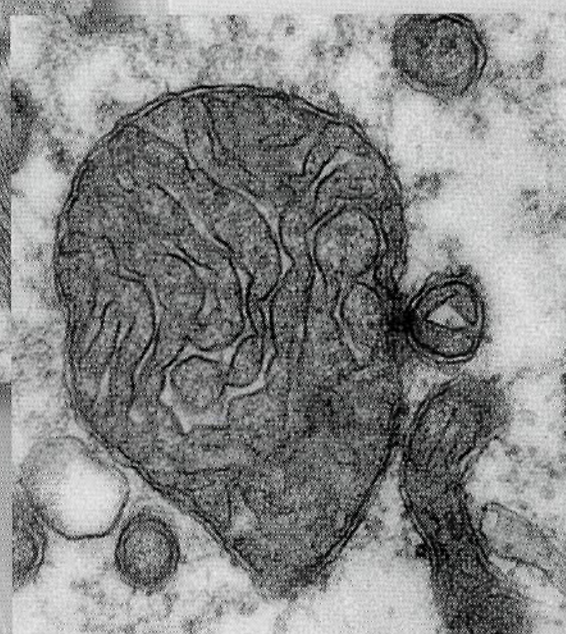

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resolution in the UHV. Therefore, SIM is potentially suitable for the characterization of ac and dc transport properties of molecular electronic circuits and nanostructures on the atomic level.

To summarize, Scanning Impedance Microscopy (SIM) is a novel microscopic technique for the characterization of transport properties that combines the spatial resolution of scanning probe microscopy with the precision of traditional impedance spectroscopy and transport measurements. SIM yields local *I-V* and *C-V* characteristics of interfaces to allow:

1. Spatially resolved resistance and capacitance measurements of individual interfaces with lateral resolution of ~50 nm or better.

2. Quantitative determination of frequency and bias dependent interface properties with very high spatial resolution and precision (compared to traditional impedance spectroscopy).

3. Elimination of contact resistances that severely limit the applicability of current sensitive techniques (both microscopic and spectroscopic). ■

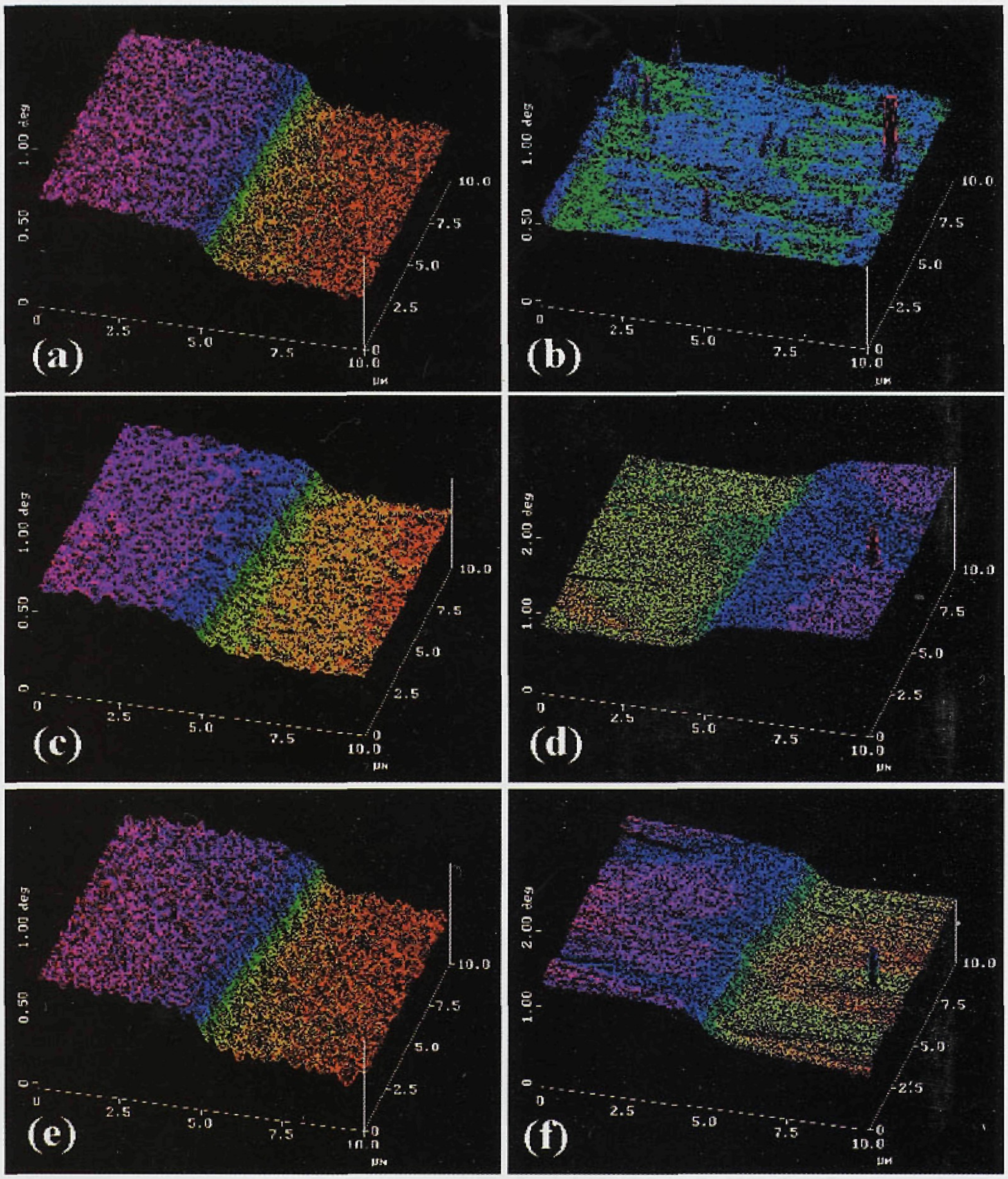

Figure 5: SIM phase (a,c,e) and amplitude (b,d,f) images of $SrTiO_3$ grain boundary in the high frequency regime under 0 V (a,b), 10 V (c,d) and -10 V (e,f) lateral dc biases. The phase change at the interface weakly depends on the lateral dc bias; *C-V* characteristic of the interface can be obtained similarly to those of the metal-semiconductor interface. No amplitude change is observed under zero dc bias condition; application of a lateral bias results in the amplitude drop across the interface. Note that surface contaminants do not influence phase image, while large topographic artifacts are observed on the amplitude image due to capacitive coupling.

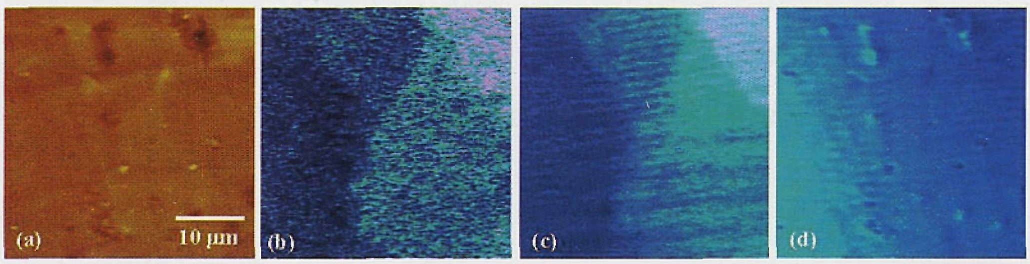

Figure 6: Surface topography (a), SIM phase image at 10 and 70 kHz (b,c) and SIM amplitude image at 70 kHz (d) for polycrystalline $BiFeO_3$ ceramics. SIM phase images directly visualize *capacitive* barriers at the interfaces, while amplitude image exhibits uniform *resistive* losses within the grains.

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