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Failure Analysis and Reliability of Low-Temperature-Grown Multi-Wall Carbon Nanotube Bundles Integrated as Vias in Monolithic Three-Dimensional Integrated Circuits

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Carbon nanotubes (CNTs) are being considered for a wide range of electronic device applications due to their high carrier mobility, high thermal conductivity, desirable mechanical and optical properties, relative ease of manufacture, and ability to carry extremely high current densities. One promising potential application for carbon nanotubes is as vias (vertical interconnects) in three-dimensional integrated circuits (3D ICs), a technology that has recently been added to the International Technology Roadmap for Semiconductors as a promising replacement for very-large-scale integration schemes.

A major challenge in the success and commercialization of 3D ICs is thermal management and fabrication of reliable via structures. To that end, our group and collaborators have demonstrated the integration of carbon nanotube vias on single-grain thin-film transistors that could be applied in a 3D IC scheme [1]. Carbon nanotubes grown at the low temperatures required for 3D ICs have higher defect concentrations and therefore higher electrical resistances than those grown at high temperatures. Therefore, the role of defects on long-term electrical reliability must be investigated.

Vias in this work were fabricated using an iron catalyst and grown at 500 °C using a top-down approach [2]. These vias display a linear current-voltage response, and a representative example cross-section image is shown in Fig 1. Testing revealed that these vias have particularly low contact resistance that is an order of magnitude less than the length-dependent resistance [3]. SEM and TEM cross-sectional imaging revealed that the very low contact resistance exhibited by these vias is likely due to the intimate physical contact between the CNT itself, metal catalyst particle embedded at the tip, and top electrode metal (Fig 2), forming a continuously conducting path to most if not all walls in the nanotube.

Ramp-to-failure reliability tests revealed that the best-performing vias outperform copper in maximum current density. The vias tested in this way break in the center of the nanotubes regardless of the final voltage at failure, which is suggestive of a Joule-heating failure mechanism (Fig 3a). The long-term stability of these structures was tested with a voltage-hold test, the results of which are shown in Fig 3b for a typical via. The resistance measured at the ramp current increased with time, more than doubling from the initial value after 24 hours. The difference between the low- and high-current resistances can be explained by self-heating in combination with negative thermal coefficient of resistance [4]. This difference increases with time. The failure mechanism of vias tested this way was the same as in the ramp to failure tests; that is, they break in the center indicating Joule heating and not electromigration is the primary failure mechanism [5].

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[5] This work is a partial contribution of NIST, an agency of the U.S government, and therefore not subject to copyright in the United States.

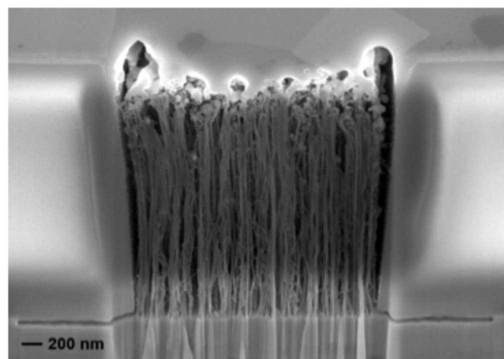

Figure 1: Cross-section SEM image (sample prepared by FIB) of a typical CNT via before testing.

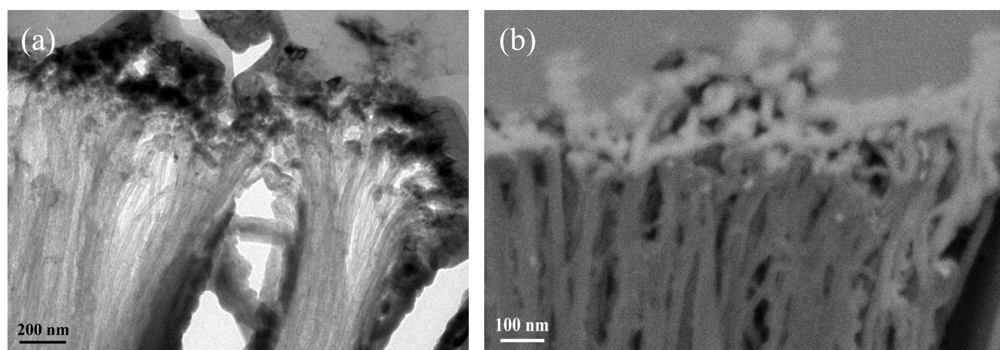

Figure 2: (a) Cross-section bright-field TEM image and (b) SEM image. Both images show the intimate contact between the CNT, catalyst at the top of the CNT, and top metal electrode that is likely responsible for the low contact resistance seen in these structures.

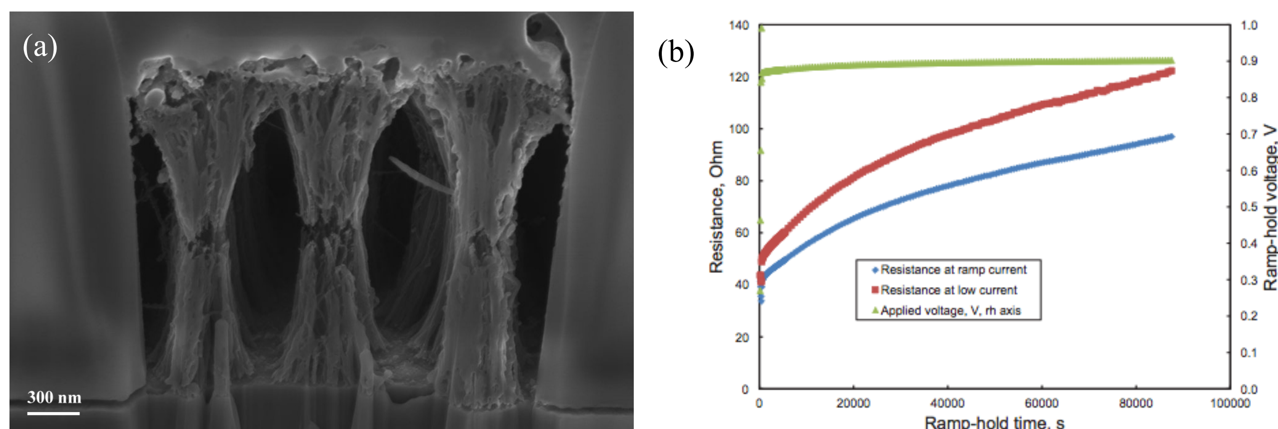

Figure 3: (a) SEM cross-section image of a representative 2 μm wide via after voltage ramp to failure testing. The tubes failed in the center, indicative of Joule heating. (b) Voltage-hold test data for a 3 μm wide via, showing that the resistance at the ramp current (lower curve) increases with time, nearly doubling over the 8.6 x 10^4 s (24 h) test interval.

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