Higher Speed Imaging: Frame Transfer CCD'S

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A number of important imaging applications, including neurobiology and precision motion analysis, require a digital camera that provides both high performance (low noise, extended linear gray scale) and high frame rates. In recent years, manufacturers have responded to this need with faster digitization/readout electronics - as high as several MHz (Mpixels/second). When combined with on-chip binning, this has enabled frame rates up to 30 frames/second from some high performance cameras. Unfortunately, even this is not fast enough for situations where two images must be acquired virtually simultaneously, or where a rapid dynamic event needs to be captured with a fast burst of images.

In this article we see how "frame transfer" architecture is able to circumvent some of the speed limitations of conventional CCDs, delivering frame rates in excess of 100 frames/second.

Several factors contribute to the overall frame rate in a typical high performance camera. These include time to open and close the shutter, image integration time and readout time. Each of these processes must occur in serial (sequential) fashion in a typical camera. The advantage of frame transfer is that it allows integration and readout to occur *simultaneously* and also permits shutter-free operation, thereby eliminating the open/close deadtime of the shutter.

How is this possible? As shown schematically in the left figure as follows, the parallel register of a frame transfer CCD consists of two distinct regions of pixels - the image, or light array and the storage, or dark array. The storage region is covered with an opaque mask; usually a thin layer of aluminum. This storage array is always situated between the image array and the serial register. In addition, the storage array is typically larger than or equal to the area of the image array.

Importantly, these two regions are controlled by two separate clocking circuits, allowing independent parallel shifting within each register. However, these circuits are controlled by the same central DSP chip and thus can be precisely synchronized.

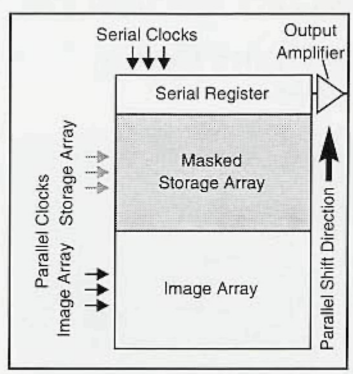
To understand the benefits of frame transfer technology, consider the simple case of acquiring two images closely spaced in time. The first image is acquired for a pre-set time on the image array. This electronic image is then rapidly shifted onto the storage array. The image array is then already accumulating another image as the storage array is sequentially read out through the serial register. In other words, image acquisition and readout may be performed simultaneously, thereby eliminating the usual readout deadtime. This capability is particularly critical in certain types of ratio imaging, where images must be acquired at two different illumination wavelengths at virtually the same instant.

This time savings is possible because the time to shift the image from one half of the parallel register to the other is much shorter than the time to readout charge through the serial register. Consider as an example the EEV37 scientific grade CCD, which has a 512 x 512 image array and a 512 x 512 storage array. The parallel register of this CCD is designed to be operated with a maximum shift rate of 3.0 microseconds/row, or 1.64 msec to shift all 512 rows. The read-out time depends on the speed of the readout electronics and whether any binning is performed; a full resolution 512 x 512 image at a 2 MHz readout rate translates into a total readout time of 0.16 seconds.

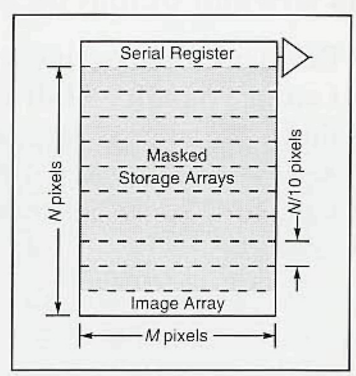
Because of the fast parallel transfer, a frame transfer camera can be operated shutterless for most applications; the integration time is usually much longer than the shift time so image smearing is negligible. This has several benefits. First the shutter open and close dead time is eliminated, which can be significant at higher frame rates. Mechanical shutters typically limit a camera to a maximum speed of around 20 frames/second. In addition, the elimination of any shutter vibrations can be a benefit when acquiring very high resolution images.

As with conventional high performance cameras, on-chip binning allows the readtime to be significantly reduced. When combined with shutterless operation, binning allows frame rates exceeding 100 frames/second for frame transfer cameras.

Frame transfer cameras also enable a rapid string of lower resolution images to be captured at extreme speeds in a so-called burst mode, which eliminates any constraints due to readout times. In this high speed framing mode, the camera optics are set up to image the scene onto a limited region of the image array, spanning say 50 rows. Now the effective image array is only 1/10 the size of the storage array. A string of 10 images can be collected and stored, limited only by the time it takes to shift 50 rows. In the case of the EEV37 array, this shift time is 150 μsec per 50 rows, allowing 10 images to be recorded in a total of 1.5 msec! ■



Frame transfer CCD



CCD masked for high speed framing

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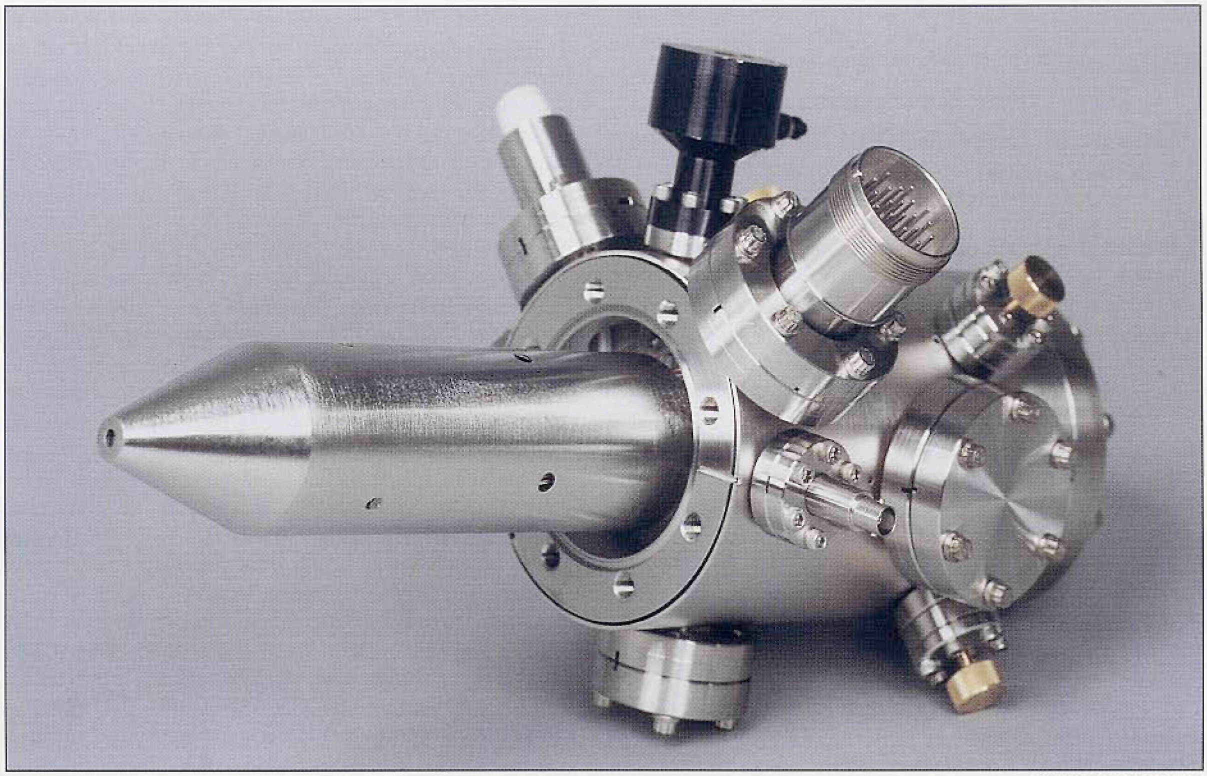

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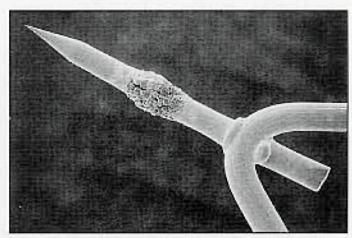

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