International Journal of Microwave and Wireless Technologies

cambridge.org/mrf

Timed array architectures and integrated true-time delay elements for wideband millimeter-wave antenna arrays

Manuel Koch, Stefan Schönhärl, Sascha Breun, Georg Fischer and Robert Weigel

Institute for Smart Electronics and Systems, Friedrich-Alexander-Universität Erlangen-Nürnberg, Erlangen, Germany

Review Paper

Cite this article: Koch M, Schönhärl S, Breun S, Fischer G, Weigel R (2025) Timed array architectures and integrated true-time delay elements for wideband millimeter-wave antenna arrays. *International Journal of Microwave and Wireless Technologies* **17**(2), 190–201. https://doi.org/10.1017/S1759078724001053

Received: 8 May 2024
Revised: 23 September 2024
Accepted: 4 October 2024

Keywords:
Beam steering; Millimeter wave integrated circuits; Phase shifters; Phased arrays; Timed arrays; True-time delay

Corresponding author: Manuel Koch;
Email: manuel.koch@fau.de

Abstract

Antenna arrays are a main driver of next generation millimeter-wave communication and radar systems as shrinking antenna sizes leverage larger arrays to compensate for reduced link budget. However, conventional phase controlled arrays exhibit a frequency dependent scan angle that appears as loss to a fixed counterpart. Bandwidth limitations introduced by the so-called beam squint effect hinder larger array sizes and data rates thereby generating a demand for timed arrays as a solution. This paper gives a quantified overview of the beam squint phenomenon, different hardware architectures as well as evaluation parameters and common shortcomings of true-time delay (TTD) elements. A broad variety of TTD realizations from literature are compared by their operational principles and performance. Finally, the delay interpolation principle, its non-idealities, and their impact on a hierarchically time delay controlled D-band antenna array are described. Extended content on a previously published, continuously tunable TTD implementation at a center frequency of 144 GHz with a bandwidth of 26 GHz and a delay range of 1.75 ps that requires only 0.53×0.3 mm^2 of core chip area is presented. Measurement results have been obtained from a demonstrator manufactured in 130 nm BiCMOS technology.

Introduction

Since demands in data rate and localization accuracy are ever increasing, next generation communication and radar systems are expected to operate in the millimeter-wave frequency range, despite higher losses and limited semiconductor performance. Reduced transmit power, increased noise floor, and smaller antenna geometries severely limit link budget and signal quality. Large antenna arrays are a promising solution to achieve higher transmit power by on-air power combining and an increase in total antenna area by combination of smaller antenna elements. Mobile communication and joint-communication-and-sensing (JCAS) applications demand quickly reconfigurable antenna arrays that support wide steering angles in order to ensure a good link quality in changing surroundings. However, large steering angles and wide bandwidths give rise to beam squinting that occurs in traditional phased arrays. Beam squinting causes the scan angle to change with frequency which can cause substantial loss due to misalignment of narrow beams across a large occupied bandwidth. Therefore, effort has been taken to develop true-time delay (TTD) elements that allow for increased instantaneous bandwidth.

At first, the chapter "Timed and phased arrays" compares the frequency dependent behavior of phased arrays with those of timed arrays and provides different approaches for timed array hardware architectures while the subsequent chapter "TTD elements" gives an overview of critical TTD metrics and operational principles. Additionally, the chapter "Delay Interpolation TTD" expands system aspects and details of our previously published work about a delay interpolation TTD in D-band [1]. Lastly, the work closes with a conclusion.

Timed and phased arrays

As shown in Fig. 1, antenna arrays can be used to emit or receive a coherent wavefront under a certain angle θ_0 if the path length difference τ_0 is compensated by delay elements. τ_0 is calculated by (1) as a function of element spacing d and scan angle θ_0. The delay difference of the outermost antennas for an N-element array is given by (2)

$$\tau_0 = \frac{d \sin(\theta_0)}{c} \tag{1}$$

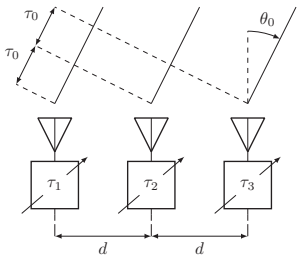

Figure 1. *N*-element antenna array under delayed excitation.

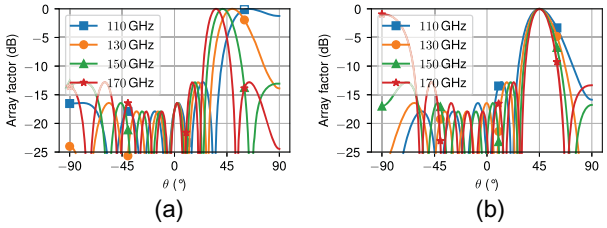

Figure 2. Array factor of an eight-element, 1 mm-spaced linear array, scanned to $\theta_0 = 45°$ at $f_c = 140\,GHz$, controlled by (a) ideal phase shift and (b) ideal TTD.

$$\tau_{0,N} = \frac{(N-1)d\sin(\theta_0)}{c}. \tag{2}$$

Beam squinting

Although the delay elements have to compensate a time delay, in practice, phase shifters are commonly used to approximate this behavior. For systems with moderate bandwidths and array sizes, this proves to be a good trade-off, due to easier realization, calibration, and especially exploitation of phase ambiguity.

However, when applied to large arrays or wideband systems, phase shifters cause significant frequency dependency of the scan angle θ_0, called beam squinting. This is due to the constant phase shift, not corresponding with the correct time delay at all frequencies of operation. Deviation of scan angle $\Delta\theta_0$ at frequency f from $\theta_{0,c}$ at center frequency f_c can be calculated using (1) and the phase shifters time delay at frequency f as shown in Equation (3)

$$\Delta\theta_0(f) = \arcsin\left(\frac{f_c}{f}\sin(\theta_{0,c})\right) - \theta_{0,c}. \tag{3}$$

As an example, an ideal 1 mm-spaced eight-element linear D-band antenna array at a scan angle $\theta_0 = 45°$ is observed. If phase shifters are used, (3) yields a beam squint of $-9.39°$ at 170 GHz and 19.15° at 110 GHz, which matches the simulated gain patterns shown in Fig. 2(a). An amplitude error of 5.1 dB, mainly dependent on the main lobe width and therefore the array size, is observed. The timed array's pattern shown in Fig. 2(b) is not affected by beam squinting and the related losses. It only shows a decreasing main lobe width at higher frequencies, which is due to the larger spacing of antenna elements d relative to the wavelength.

Instantaneous array bandwidth

For communication systems, the demonstrated amplitude loss due to beam squinting is of main interest as it directly affects the channel response. The normalized array factor and therefore also the frequency response of a phase controlled linear array is given

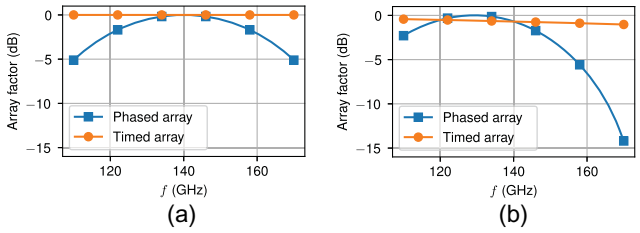

Figure 3. Array factor of an eight-element, 1 mm-spaced linear phased / timed array over frequency, steered to $\theta_{0,c} = 45°$ and received at (a) 45° and (b) 50°.

by (4) [2]. Figure 3(a) shows the example case's array factor frequency response at $\theta_0 = 45°$ that exhibits a loss of 5.1 dB at the band edges which matches the previous observations of Fig. 2(a). The phase response does not contain any phase or group delay distortions as it does not deviate from an ideal time delay which is 0 , if phases are referred to the center element

$$AF_n = \frac{1}{N}\left(\frac{\sin\left(\frac{N}{2}\psi\right)}{\sin\left(\frac{1}{2}\psi\right)}\right),\ \psi = \frac{2\pi f}{c}d\,cos\theta + 2\pi f_c\tau_0. \tag{4}$$

A phased array's 3 dB bandwidth can be directly calculated from (5), resulting in 46.99 GHz for the uniformly illuminated case (beam broadening factor $B_b \approx 1$) [3]

$$BW_{ps,arr,3dB} = \frac{0.886B_bc}{Nd\sin(\theta_0)}. \tag{5}$$

Considering the applicability of phased arrays to millimeter-wave transmitter systems, a misalignment between beam direction and actual placement of the receiver must be taken into account. Figure 3(b) shows the normalized array factor over frequency if the receiver is located at an angle of 50° while the phase shifters are still configured for 45°. As some of the beams in Fig. 2(a) have a steep slope at 45°, a drastic increase in loss is observed, while only little additional loss is caused by the timed array.

Intersymbol interference in phased arrays

In phased arrays, only carrier phases are aligned using a constant phase shift which has no influence on the group delay and therefore the signal envelope remains unaffected. Thus, phased array imperfections under perfect beam alignment can be also described by the envelope delay difference τ_0 between elements. This effect causes intersymbol interference (ISI), similar to multipath propagation, with a maximum path length difference of $(N-1)\tau_0$, degrading error vector magnitude of digitally modulated signals.

A mitigation technique, including a case study for 5G signals, using digital equalization is thoroughly described in [4]. In the course of this work a simulation model closely following [4] has been created as shown in Fig. 4(a) which is applied to the previous example case. The model passes a 60 GSa/s sampled impulse through a root-raised-cosine filter, N different delays, representing the phased array, and another root-raised-cosine filter to be finally processed by a $N+1$ tap linear equalizer.

As expected, Fig. 4(c) shows that the distortion introduced by the array is compensated by the equalizer. Transformation into frequency domain, depicted in Fig. 4(d), further shows that the array factor loss described by this model coincidences well with the calculations of the previous section. From the frequency response, it

https://doi.org/10.1017/S1759078724001053 Published online by Cambridge University Press

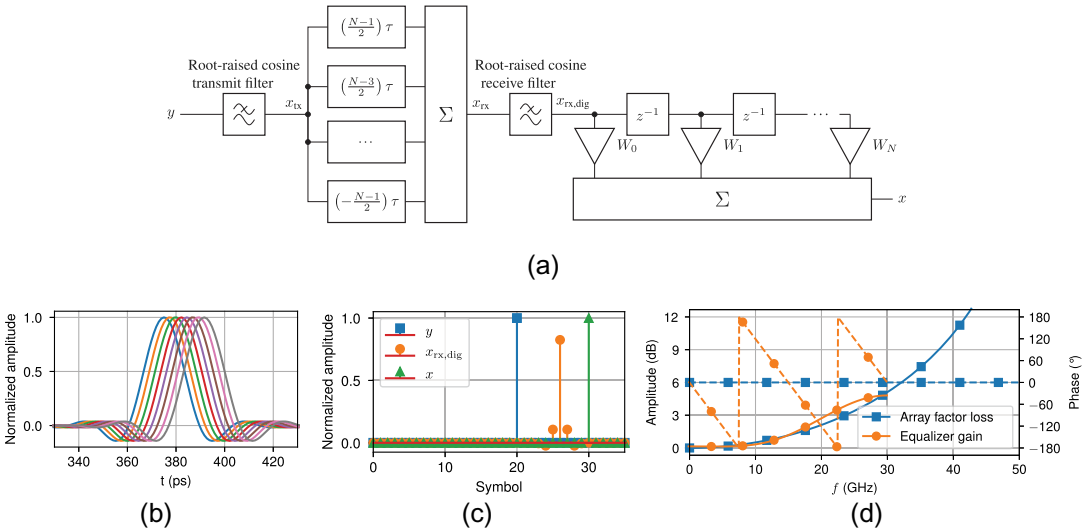

Figure 4. (a) Baseband phased array model with equalizer, (b) intersymbol interference of shaped and delayed impulses, (c) impulse response of undistorted, distorted, and equalized signals in digital baseband, and (d) amplitude (solid) and phase response (dashed) of $\frac{x_{\mathrm{tx}}}{x_{\mathrm{rx}}}$ and the equalizer taps.

is also apparent that the equalizer compensates the losses of the phased array and additionally introduces a constant delay of four symbol periods. However, as the equalizer operates in digital baseband it requires sufficient power amplifier back-off respectively signal-to-noise ratio to compensate the loss of array gain, which makes it suitable if moderate loss is introduced by beam squinting. If link budget is more severely degraded, the use of timed arrays instead of phased arrays might be a better option to completely avoid beam squinting.

Array architectures

Phase ambiguity greatly simplifies the realization of phased arrays over timed arrays as covering a certain delay range is not an issue and amplitude calibration can be directly implemented by vector phase shifters. In contrast, TTD elements often have limited delay range, finite resolution, bigger size and are generally more expensive, which lead to the development of several approaches for combining TTD elements with phase shifters.

One approach is to use a dedicated control path for every antenna element, e.g. phase shifter, TTD element, or a cascade of both. References [3, 5] give a detailed description of array pattern errors due to periodic control errors, e.g. introduced by quantized phase shift or TTD that causes a triangular delay error over M_{Q} antenna elements until $M_{\mathrm{Q}}\tau_0$ is a multiple of the delay element's least significant bit (LSB). The introduced error can be modeled as subarrays with M_{Q} elements whose scan angles deviate from the intended scan angle θ_0. Thus, the zeros of the M_{Q}-element subarray patterns do not align with the lobes of the array of subarrays which is why quantization lobes appear in the array pattern. The first order quantization lobes occur at an angle of $\theta_{\mathrm{Q}} = \arcsin\left(\sin(\theta_0) \pm \sin(\frac{c}{fM_{\mathrm{Q}}d})\right)$ and have a level according to (6). The worst case level is reached for $M_{\mathrm{Q}} = 2$ which is the case if the delay between contiguous antenna elements is $\tau_0 = 1.5\tau_{\mathrm{LSB}}$ [3]

$$QL_{\mathrm{dB}}/(\mathrm{dB}) \lesssim 4 - 6.02N,\ N = -log_2(f\tau_{\mathrm{LSB}}) \geq 3. \qquad (6)$$

A second approach is to partition larger timed arrays into smaller, sufficiently wideband, phase controlled, contiguous subarrays that are time controlled at their subarray ports. This approach increases the bandwidth according to (5) by a factor equal to the number of M-element subarrays Q, compared to a purely phase controlled array, effectively replacing N by M in (5). As beam squinting causes the M-element phased subarrays' scan angle to deviate from the intended angle, sidelobes appear. As the number of elements M is given by geometry, the lobes' angles can be calculated analogously, whereas the pth lobe level is computed by (7) [3]

$$P_L = \frac{\pi^2\left(\frac{d}{c}\Delta f \sin\theta_0\right)^2}{\sin^2\pi\left(\frac{d}{c}\Delta f \sin\theta_0 + \frac{p}{M}\right)}. \qquad (7)$$

Additionally, quantized TTD at the subarray ports generates another level of subarray grouping with a periodicity of $M_{\mathrm{sQ}}M$ antenna elements. Quantization lobe levels can be calculated with the same formula by treating the M-element phase controlled subarrays as antenna elements, which reduces the quantization lobe level due to multiplication with the subarray pattern [3, 5]. As the periodicity $M_{\mathrm{sQ}}Md$ is spatially larger than Md, these quantization lobes are closer to θ_0 than the beam squint lobes. However, if quantization errors are known and reduced quantization lobes can be tolerated at off-center frequencies, one may consider to use the subarrays' phase shifters to increase the TTD resolution without additional hardware effort.

For mitigation of these grouping effects like the mentioned peak sidelobes or the beam pointing error, several techniques such as randomization, rounding off, or overlapping subarrays are described in literature [3, 6].

Delay integration in frequency converter

Unlike phase shifters that can be reasonably used in the local oscillator (LO) path, TTD has to be integrated into the signal path to benefit from its frequency dependent phase response. Considering the two mixing products of an up-conversion mixer, described by basic addition theorems as shown by (8), alternative concepts to radio frequency (RF) path time delays can be derived. Both mixing products can be phase shifted in the LO and

https://doi.org/10.1017/S1759078724001053 Published online by Cambridge University Press

Table 1. Equivalent RF delay type of frequency converter integrated delay elements

Architecture	IQ/DSB modulation	SSB modulation
IF PS	–	Phase shift
IF PS & IF TTD	–	Time delay
LO PS	Phase shift	Phase shift
LO PS & IF TTD	Time delay	Time delay
LO PS & RF GTD	Time delay	Time delay
RF PS	Phase shift	Phase shift
RF TTD	Time delay	Time delay

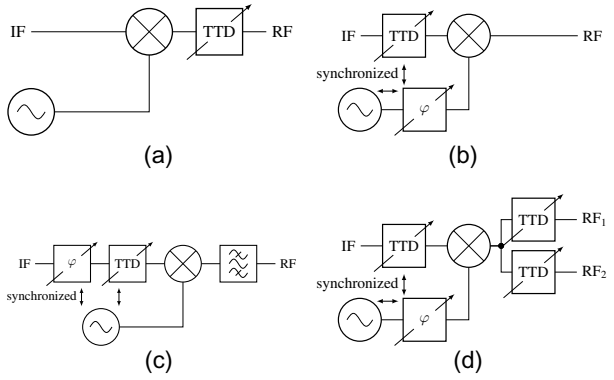

Figure 5. Timed array system concepts using (a) RF TTD, (b) IF TTD and LO phase shifter, (c) IF phase shifter and TTD for SSB systems, and (d) combined concepts for hierarchical delay concepts.

intermediate frequency (IF) path as well as time delayed in the IF path

$$s_{\mathrm{RF}}(t) = \cos\left(\omega_{\mathrm{LO}}t + \varphi_{\mathrm{LO}} + \omega_{\mathrm{IF}}t + \omega_{\mathrm{IF}}\tau_{\mathrm{IF}} + \varphi_{\mathrm{IF}}\right) + \cos\left(\omega_{\mathrm{LO}}t + \varphi_{\mathrm{LO}} - \omega_{\mathrm{IF}}t - \omega_{\mathrm{IF}}\tau_{\mathrm{IF}} - \varphi_{\mathrm{IF}}\right) \quad (8)$$

$$\varphi_{\mathrm{RF,USB}} = (\omega_{\mathrm{LO}} + \omega_{\mathrm{IF}})\tau_{\mathrm{RF}} \overset{!}{=} \varphi_{\mathrm{LO}} + \omega_{\mathrm{IF}}\tau_{\mathrm{IF}} + \varphi_{\mathrm{IF}} \quad (9)$$

$$\varphi_{\mathrm{RF,LSB}} = (\omega_{\mathrm{LO}} - \omega_{\mathrm{IF}})\tau_{\mathrm{RF}} \overset{!}{=} \varphi_{\mathrm{LO}} - \omega_{\mathrm{IF}}\tau_{\mathrm{IF}} - \varphi_{\mathrm{IF}}. \quad (10)$$

Several possible approaches are listed in Table 1 and shown in Fig. 5. A linear phase over frequency can be achieved by shifting LO and delaying IF, which is equivalent to an RF path time delay and can therefore be used for all modulation types including in-phase quadrature (IQ) and double sideband (DSB) modulation. In this context, a group time delay (GTD), e.g. [7], in the RF path has the same effect as the IF TTD. Assigning the delay functionality completely to the IF path works only for single sideband (SSB) systems, as the second mixing product will be shifted by the inverse IF phase, which is only acceptable if it is discarded. As depicted in Fig. 5(d), functionality can be also combined to achieve subarray and element level controls. It is noted that this combination does not introduce the grating lobes discussed in the previous subsection since TTD is used for element level control.

TTD elements

This section gives an overview of relevant properties and requirements of TTD elements as well as implementation methods. Practical TTD element properties include phase properties (delay range, flatness of phase/group delay as well as resolution, accuracy and precision of delay control), amplitude properties (gain/loss, bandwidth, gain error over delay setting), and other parameters (power consumption, chip area). TTD implementation methods, grouped into switch-based TTD, switch integrated TTD, and continuously adjustable TTD, are presented in subsection "Operational principles and realizations".

TTD specifications

TTD elements have to have a bandwidth which is superior to the beam squint induced bandwidth $BW_{\mathrm{ps,arr,3dB}}$ given by (5) while providing sufficient delay range $\tau_{0,N}$ to cover N antennas as given by (2), in order to reduce the bandwidth limitations of phased arrays. As both parameters depend on the array size, the phased array's bandwidth can be approximated by (11), only using $\tau_{0,N}$ and the beam broadening factor B_{b} as variables. Accordingly, Fig. 6 compares the absolute bandwidth of TTD realizations with the calculated phased array bandwidth. At this point, it is noted that the comparison is not perfectly fair as the publications use different definitions of bandwidth, e.g. measurement graphs in [8] indicate less than 3 dB gain variation over the characterized D-band while [9–12] exhibit a significant negative gain slope

$$BW_{\mathrm{ps,arr,3dB}} \overset{N\approx(N-1)}{\approx} \frac{0.886B_{\mathrm{b}}}{\tau_{0,N}}. \quad (11)$$

From Fig. 6, it is apparent that many TTD realizations with small delay ranges possess a smaller 3 dB bandwidth than conventional phased arrays. When considering hybrid architectures using phase controlled subarrays, due to sufficient bandwidth, beam squint induced sidelobes must be also taken into account. For example, according to (5), four-element, 1 mm-spaced phased subarrays at 140 GHz and $\theta_0 = 45°$ still have a bandwidth of almost 94 GHz, but beam squinting causes lobes up to −15.0 dB for a bandwidth of ±15 GHz and −7.6 dB for ±30 GHz according to (7). Acceptable sidelobe levels depend on the targeted application, but high sidelobes may be problematic for radar applications and communication systems featuring JCAS functionality. A considerably higher bandwidth-delay-product is achieved by moderate frequency, high bandwidth designs up to 50 GHz [9] and 21 GHz

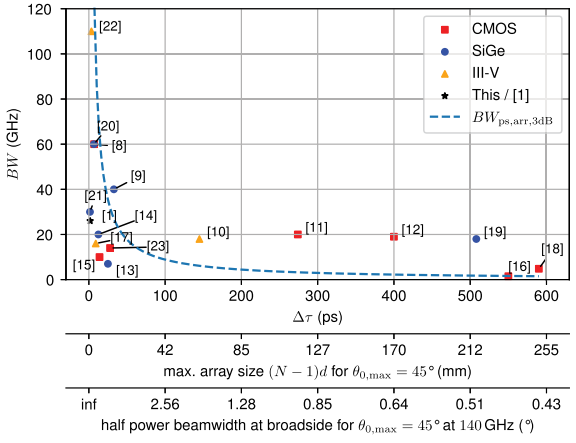

Figure 6. Bandwidth of TTD realizations [1, 8–23] versus their delay range compared with the phased array bandwidth approximated by (11). Maximum array size and half-power beamwidth (HPBW) related to $\Delta\tau$ according to (2) and (13) [3] are shown as additional axes for $\theta_{0,\max} = 45°$ at 140 GHz.

https://doi.org/10.1017/S1759078724001053 Published online by Cambridge University Press

[10–12, 19] that can also be used for sub-THz systems when employed in the IF domain as discussed in Section "Timed and phased arrays".

TTD elements are expected to avoid beam squinting over a certain bandwidth by providing a constant phase delay τ and therefore a linear phase $\varphi = -\omega\tau$. Correct group delay is not a sufficient criterium for the beamforming functionality as it defines only the slope of the phase. The remaining beam squint due to a deviation of phase and group delay of all-pass delay cells is examined in [24]. Normally, the relative delay compared to a reference state is of interest as it also describes the tuning range at the antenna port. Referring the forward transmission coefficient S_{21} of delay setting B to that of a reference state also removes most of the phase ambiguity and allows easy extraction of relative phase delay and gain variation

$$S_{21,\mathrm{n}}(f, B) = \frac{S_{21}(f, B)}{S_{21}(f, B_{\mathrm{ref}})}. \tag{12}$$

The resolution of TTD should be high enough for scanning the beam in steps that are smaller than the beamwidth. The smallest step of θ_0 in fractions of the half-power beamwidth (HPBW) is given by (14) which is derived from (2) and the left of (13) [3] as a function of the LSB of the delay $\tau_{0,N}$. For a certain τ_{LSB}, smaller steps of the scan angle θ_0 and reduced HPBW of large arrays cancel each other, giving a constant result. This expression is optimistic as the HPBW can be reduced by element patterns and $\Delta\theta_0$ increases with θ_0. Further, quantization of intermediate elements is ignored that causes the formation of subarrays

$$HPBW = \frac{0.886 B_b \lambda}{Nd} \overset{N\approx(N-1)}{\approx} \frac{0.886 \sin\theta_{0,\max}}{f\tau_{0,N}} \tag{13}$$

$$\frac{\Delta\theta_0}{HPBW} \overset{N\approx(N-1),\, \sin\theta_0\approx\theta_0}{\approx} \frac{\tau_{\mathrm{LSB}} f}{0.886 B_{\mathrm{b}}}. \tag{14}$$

Therefore, another criterion is the level of quantization sidelobes. The worst-case level is approximately given by (6) and applies to element level control as well as timed control at the subarray ports of subarrays. Figure 7 compares both criteria with TTD realizations that have non-continuous control of delay. Realizations at D-band frequencies provide enough resolution for approximately 20 dB of quantization lobe rejection. In the case of a quantized IF path TTD element and high resolution phase shifter, the resulting delay is $\tau_{\mathrm{RF}} = \frac{\omega_{\mathrm{LO}}\tau_{\mathrm{LO}}}{\omega_{\mathrm{RF}}} \pm \frac{\omega_{\mathrm{IF}}\tau_{\mathrm{IF}}}{\omega_{\mathrm{RF}}}$ and therefore the LSB at the RF port can be calculated to $\tau_{\mathrm{LSB,RF}} = \frac{\omega_{\mathrm{IF}}}{\omega_{\mathrm{RF}}}\tau_{\mathrm{LSB,IF}}$. Consequently, the resolution requirements of IF path TTD is determined by the IF frequency and not the RF frequency. This means that the resolution in phase matters, not in time. In Fig. 7, it can be seen that many lower frequency implementations also achieve 20 dB quantization lobe suppression, while some of the not shown designs implement continuous high resolution stages [9, 12–14, 23, 26, 27].

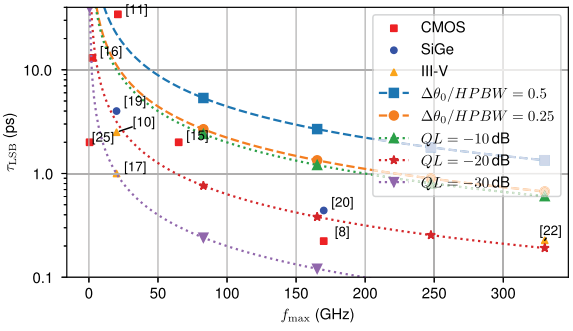

Figure 7. Least significant bit (LSB) of delay $\Delta\tau$ of TTD realizations [8, 10, 11, 15–17, 19, 20, 22, 25] versus their maximum operational frequency compared with the criteria of sub-HPBW resolution, according to (14), and quantization lobe *QL* suppression according to (6).

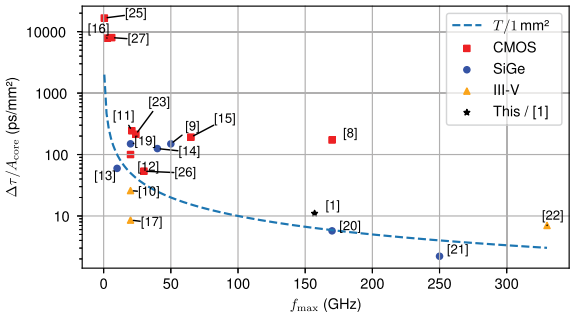

Figure 8. Delay range per core area of integrated TTD elements [1, 8–17, 19–23, 25–27] versus their maximum supported frequency and a trendline indicating one period per square millimeter.

Errors of phase and amplitude at the antenna ports generally cause directivity degradation, pointing error and grating lobes. If errors are periodic, strong sidelobes are expected, whereas random errors cause an increase of the average sidelobe level [3]. However, a linear amplitude taper due to an expected correlation of loss and delay showed little effect on the peaks of the sidelobes of a rectangular taper, but hinders complete extinction of the array factor's exponential terms with 180° phase difference.

In contrast to phase shifters which exploit the ambiguity of a periodic signal for large phase differences, TTD elements have to incorporate spacious delay elements. Therefore, a critical parameter is the required chip area for a certain delay. Figure 8 charts the delay range per chip area over the maximum operational frequency. Implementations at lower frequencies tend to achieve a higher delay range per area compared to higher frequency implementations as less wideband design options like (active) filters [11, 12, 14, 16, 18], artificial transmission lines (ATLs) [8, 9, 19], and compact switches are available. In contrast, the mm-wave designs [20–22] use conventional transmission lines and area inefficient $\lambda/4$ transformed shunt switches. Paper [8] achieves a much higher area efficiency as series CMOS switches are used and $\lambda/4$ lines are mostly avoided. The general trend can be empirically approximated by a delay of one period per square millimeter.

Operational principles and realizations

TTD elements covering large time delays typically involve switches and constant delay elements as this technique offers low losses for large delays and well-predictable delay steps. Table 2 gives an overview of constant delay elements like lumped filters [11, 12, 14, 16, 18] that are highly efficient regarding chip area per delay but are limited to low frequencies compared to artificial transmission lines (ATLs) [8, 9, 19] or transmission lines (TLs) [1, 20–22]. Switching between different delays can be accomplished by selecting the desired tap of a delay chain [9, 14, 16, 18], posing the problem of imperfect matching at higher frequencies, making techniques, e.g. as described by [9] necessary. Another special case is the trombone architecture that incorporates a forward and reverse traveling signal line with switched amplifiers that

https://doi.org/10.1017/S1759078724001053 Published online by Cambridge University Press

Table 2. Integrated TTD elements by operational principle

Path switching time delay elements		f_{max}
Allpass/lowpass filter	[10–12, 16, 18] / [14]	40 GHz
Artificial transmission line (ATL)	[8, 9, 19]	170 GHz
Transmission line (TL)	[1, 20–22]	330 GHz
Delay chain selection	[9, 10, 14, 16, 18]	50 GHz
Trombone architecture	[8, 11, 12]	170 GHz
Delay bypassing	[19–22]	330 GHz
Switch integrated delay elements		
Self-switched constant-R network	[8, 10, 12]	170 GHz
Reflective switched transmission line	[23]	24 GHz
Switch tuned allpass filter	[16]	2.5 GHz
Switch tuned TL/ATL	[15]	65 GHz
Continuous delay elements		
N-path sample and hold	[25, 27]	6 GHz
Reflective tuned transmission line	[23]	24 GHz
Tuned capacitance allpass filter	[12, 13]	20 GHz
Varactor tuned TL/ATL	[9, 14, 17]	50 GHz
Coupled transmission line	[26]	30 GHz
Delay interpolation	[1]	157 GHz
Vector phase shifter	[21]	250 GHz

select the point of return [11, 12]. If switches are used instead of amplifiers, impedance matching at the point of return must be assured which requires a high impedance state of the remaining TLs. This can be achieved by shorting the lines $\lambda/4$ after the point of return [8]. Another switch-based architecture is bypassing of individual (binary weighted) delays using dual SPDT switches [19–22]. As series transistor switches are difficult to realize at very high frequencies, some millimeter-wave implementations use $\lambda/4$ transformed shunt switches [20–22]. To accommodate for the parasitic elements of switches, some designs integrate switch and delay element, resulting in self-switched all-pass networks [8, 10, 12]. Reflective type delay elements require directional couplers but allow delay selection by shorting the signal to ground or even employing offset shorts for better delay resolution [23].

Most of the presented principles are not very suitable for small delay steps as the high amount of switches requires a large chip area and increases parasitic capacitance that limits the maximum frequency. Similar to a ring buffer, many sample and hold circuits can be used to temporarily save the input signal and delay the output signal [25, 27]. However, to cover higher frequencies, the resolution of lumped filters and reflective delays can be improved by integrating digitally controlled capacitors [16] or varactors [12, 13, 23]. The same technique is applicable to ATLs and TLs, but a trade-off between pole frequency, impedance matching, tuning range, and variation of the capacitor's quality factor and therefore loss variation across delay setting has to be found, which is increasingly difficult at higher frequencies [9, 14, 15, 17]. Some designs also incorporate tunable inductors to preserve impedance matching over delay [15]. A less intuitive approach is to exploit different propagation speeds in common and differential mode of coupled lines. By injecting an amplitude controlled copy of the signal in the second path, modes can be changed and therefore the delay of the line. This technique is limited in its maximum delay by power transfer and therefore gain variation over delay setting [26]. An alternative to high resolution TTD are conventional phase shifters with limited tuning range, combined with a coarse TTD element, causing only negligible beam squinting [3, 21]. The delay interpolation principle employed in this work is similar to a vector phase shifter, but instead of a 90° hybrid, a TL is used, which allows for continuous delay control by interpolation [1].

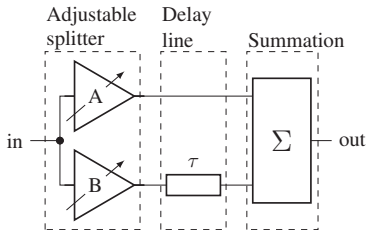

Figure 9. Delay interpolation TTD principle.

Delay interpolation TTD

Analysis of TTD requirements and the state of the art showed the need for both, high delay range TTD implementations for steering large arrays, but also high resolution methods that allow a high suppression of sidelobes, necessary for upcoming radar and JCAS mm-wave systems. Loss and capacitances of series switches in the mm-wave regime make it difficult to cascade switches or design ATLs with high enough impedance and cut-off frequency for the realization of small delay steps, although respectable results are achieved using advanced CMOS processes [8]. However, so far BiCMOS realizations [20, 21] employ spacious $\lambda/4$ transformed shunt switches that require an increasing portion of the TTD element's chip area as delay steps are reduced. Phase shifters using Lange couplers have already been used to increase the resolution [21]. In [1], we proposed a TTD design that is similar to a vector phase shifter but uses a delay line instead of a 90° hybrid. Figure 9 illustrates the working principle that utilizes a continuously adjustable splitter for generating an undelayed and a delayed signal portion that are combined by a summation stage. This scheme provides continuous delay interpolation with a delay range of τ without the need for RF switches.

As described in our previous work [1], gain and phase characteristics can be calculated by vector addition of the two portions with one of them being delayed by the time τ according to (15). To limit the output amplitude to 1, the sum of both weights A and B is set to 1

$$H(\omega) = A + Be^{-j\omega\tau},\ A + B = 1. \tag{15}$$

Calculating the phase response yields (16) which approximates a linear tuning behavior as long as the phase difference of both signals is small. Due to the constant delay τ, the phase difference increases with frequency, which causes a deviation $\Delta PD/\tau$ from the linear behavior. Figure 10(b) shows how the error increases as the signal period T approaches the delay τ

$$\phi = \arctan\left(\frac{B\sin(-\omega\tau)}{(1-B)+B\cos(-\omega\tau)}\right) \approx B(-\omega\tau) \tag{16}$$

$$PD = -\frac{\phi}{\omega} \approx B\tau. \tag{17}$$

https://doi.org/10.1017/S1759078724001053 Published online by Cambridge University Press

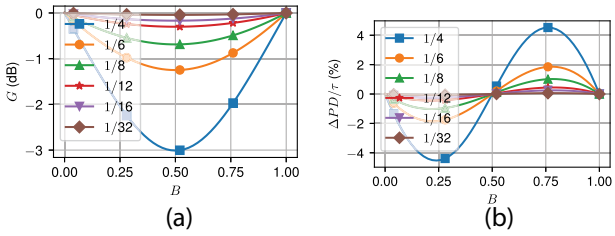

Figure 10. (a) Gain variation and (b) deviation from linear delay of the delay interpolation TTD over delay setting B for different delay to signal period ratios τ/T.

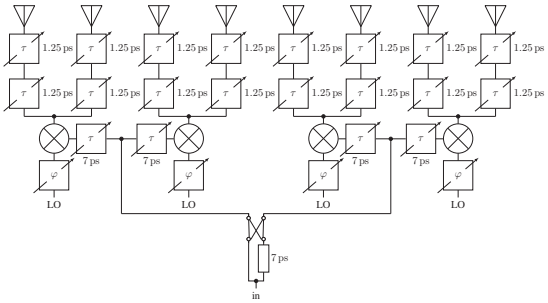

Figure 11. An eight-element linear antenna array controlled by a three-level hierarchical beamforming network.

As the phase difference increases with frequency the sum of both vectors is reduced at higher frequencies which causes a low-pass behavior that is dependent on the delay setting. As shown in Fig. 10(a), the highest loss occurs at $A = B = 0.5$ which can be calculated from (18)

$$G_{\mathrm{dB}}(B = 0.5)/(\mathrm{dB}) = 20\log_{10}\left(\cos\left(\pi\frac{\tau}{T}\right)\right). \qquad (18)$$

As gain and phase imperfections depend on the signal period T, the TTD element can only be used up to a certain frequency, e.g. $\tau = \frac{1}{4f_{\max}}$ results in a gain variation of up to 3 dB.

Hierarchical beamforming systems

This section describes a concept for a completely time delay controlled array that can be realized using the delay interpolation principle. Because, according to (2), the required delay range increases linearly with array size, the hierarchical architecture shown in Fig. 11 is proposed to benefit from the typically higher delay ranges of baseband TTD elements. As continuously adjustable TTD elements are utilized, no grating lobes due to quantization or beam squinting are expected, yet some deterioration, e.g. due to gain variation or tuning non-linearity is expected.

The required element-to-element delay of a 1 mm-spaced antenna array for $\theta_0 = 45°$ in D-band is calculated by (1) as $\tau_0 = 2.35$ ps and has to be available for controlling the two-element subarrays. Two cascaded TTD elements for subarray beamsteering in the RF domain are proposed to meet the required tuning range while reducing the loss at $B = 0.5$ in comparison to a single element. As the distance and therefore also the required delay between the subarray ports is 6 times higher, a combination of baseband TTD and LO phase shifting becomes more attractive. For zero-IF systems, the highest frequency that the TTD element has to support is $\frac{BW}{2}$ instead of $f_{\mathrm{LO}} + \frac{BW}{2}$ which increases the achievable delay range of delay interpolation TTD by a factor of 5.6 for

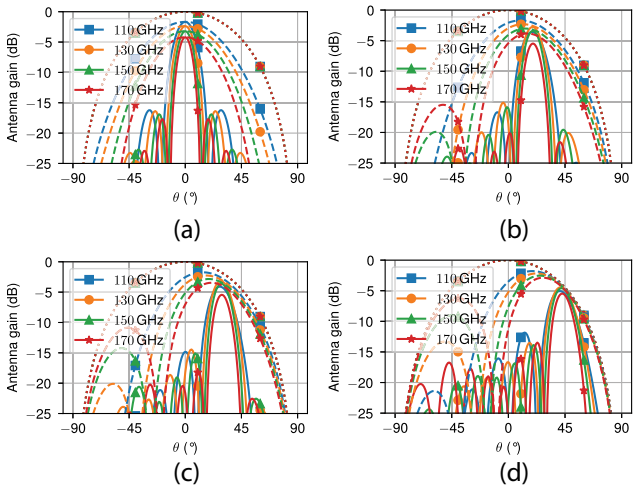

Figure 12. Gain of a cosine modeled antenna (dotted) and the hierarchical timed array architecture for the two-element subarrays (dashed) and the complete eight-element array (solid) at scan angles θ_0 of (a) 0°, (b) 20°, (c) 30°, and (d) 45°.

the D-band example. Due to the increased delay range of 7 ps for the continuous delay elements, a single fixed 7 ps delay element with crossover switch is sufficient for preserving continuous delay control. If the fixed delay element is switched to either side, the delay can be compensated by the continuous elements on the other side, yielding $\theta_0 = 0°$, or increased by the elements on the same side, which defines the maximum scan angle $\theta_{0,\max} = 45°$ since $6\tau_0 \approx 2 \cdot 7$ ps. For scanning the other half of space, the crossover switch has to be toggled. The use of baseband TTD appears further attractive because area efficiency may be increased by replacing spacious inductive matching networks with resistors due to higher gain and efficiency at lower frequencies. Depending on the chosen architecture, gain variation may also be improved by lower losses of long delay lines and switches.

The timed array's gain has been simulated for a cosine modeled element pattern, appropriately switched delay element and by using the transfer function of the delay interpolation TTD element (15) with B determined by (17) without applying further compensation. Figure 12 shows the element pattern together with the wide patterns of the subarrays and the narrower patterns of the overall eight-element array. The frequency dependent gain variation due to the RF TTD element becomes apparent for $B_{\mathrm{TTD,RF}} = 0.5$ at $\theta_0 = 0°$ where significant deviation between element and subarray pattern can be seen, while at higher scan angles the RF TTD elements operate closer to the extreme settings where less losses occur. At $\theta_0 = 20°$, gain variation of the baseband TTD elements cause a reduced gain of the array pattern compared to the subarrays' pattern towards the band edges. The influence of gain variation on the array gain shows the need for hardware-based gain compensation or a control-based reduction, e.g. by avoiding the central control setting in a chain of cascaded delay interpolation TTD elements.

D-band implementation

Previously, we presented a D-band TTD design to evaluate the feasibility of the delay interpolation working principle, circuit non-idealities, and compensation techniques [1]. The design as well as additional investigations regarding the non-idealities are presented in the following section. The implementation closely follows the topology shown in Fig. 9. As the output power at low frequencies

https://doi.org/10.1017/S1759078724001053 Published online by Cambridge University Press

and extreme delay settings is nearly equal to the sum of A and B, their sum is kept constant by splitting the input signal into parts A and B. For this purpose, the architecture of a conventional cascode current steering variable gain amplifier is slightly altered to realize an adjustable splitter, shown in Fig. 14(b), that keeps the overall power of both signals constant, but divides them into two weighted components. The ratio of both signals can be controlled by potentials c_1 and c_2, which are set by a differential current mode digital-to-analog converter (DAC). Ideally, the input conductance of the splitting stage is constant as it is $g_1 + g_2 = \frac{I_1}{V_T} + \frac{I_2}{V_T}$ with the sum of the collector currents $I_1 + I_2$ and the thermal voltage V_T being constant. However, high frequency designs commonly use small transistor sizes to reduce parasitic capacitance which increases undesired series resistance. If the splitting stage's input admittance g_s is modeled by (20) using the transistors' small signal conductances, an emitter series resistance $R_E = 9.6\,\Omega$ and an RC network, representing parasitic coupling from emitter to collector, a non-constant input admittance is obtained as shown in Fig. 13(a). Good agreement between simulation and calculation at DC is observed, while at the center frequency of 145 GHz parasitic

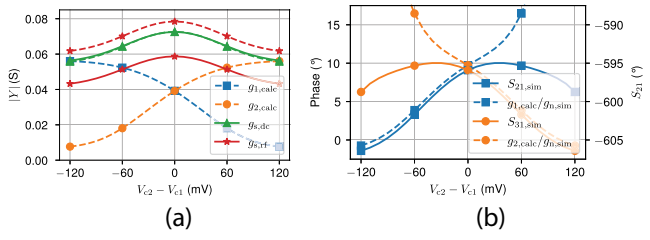

Figure 13. Simulated (solid) and calculated (dashed) (a) splitting stage input admittance g_s at DC and center frequency, individual emitter admittances g_1, g_2, (b) simulated phase of the complete splitter circuit S_{21}, S_{31} (right axis) and phase from the ratio of calculated g_1, g_2 and simulated admittance of the splitting stages input node g_n.

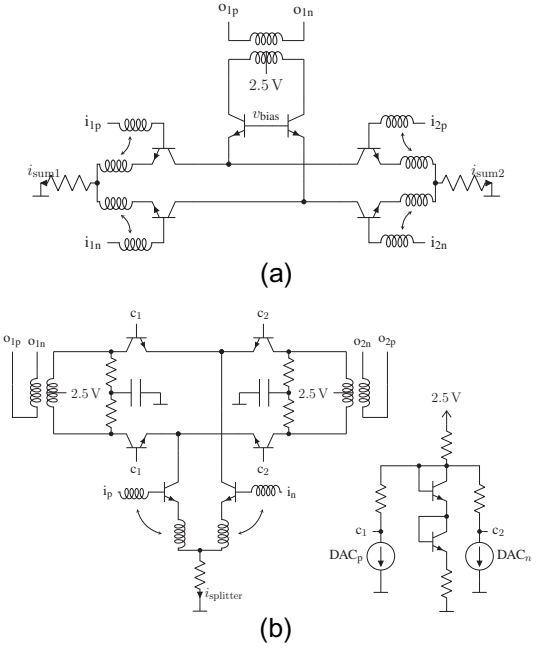

Figure 14. Simplified schematics of (a) the summation circuit and (b) the adjustable splitter with control network.

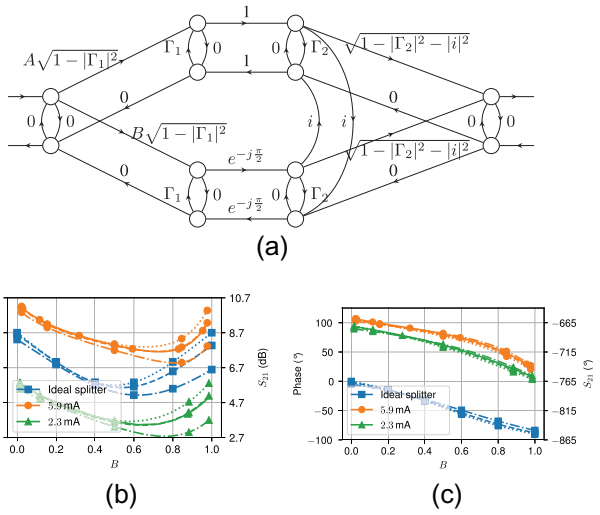

Figure 15. (a) Signal-flow graph considering reflections at the splitter's outputs (Γ_1), the summation circuit's inputs (Γ_2), and isolation of the summation circuit (i). (b) Simulated gain at 140 GHz of the TTD circuit with lossless delay lines (solid, right axis), calculated gain using simulated reflection parameters and isolation (dashed), calculated gain without reflections and infinite isolation (dotted), calculated gain with 10 dB matching and 10 dB isolation (dash-dotted) for an ideal splitter and different splitter bias currents, and (c) phase responses for the same cases.

elements cause a higher deviation. Further, the ratio of g_1, respectively g_2, and the splitting stage's simulated input node admittance $g_{n,sim}$ is used to estimate phase errors introduced by the power splitter. Figure 13(b) compares them with the simulated S-parameters of the complete splitter circuit. In the regions of high gain, a good accordance is observed while at low gain the phase is sensitive to the transistors' isolation properties, which are only coarsely modeled by the simple RC network

$$g_i = \frac{1}{R_E + \frac{V_T}{I_i}} + \frac{1}{60\,\Omega + \frac{1}{j\omega 7.6fF}} \tag{19}$$

$$g_s = g_1 + g_2. \tag{20}$$

The splitter's matching is realized with coupled inductors at the input and transformers at the output, both optimized for a center frequency of 145 GHz.

Two differential TLs with a delay difference of 1.78 ps are used as delay element which provide a well-predictable delay and simplified routing. As the length difference of the TLs reaches 90°, imperfect matching and impedance transformation along the delay line cause asymmetry in the amplitude response. The signal-flow path shown in Fig. 15(a) is used to quantify the effect of reflections at the splitter's outputs and the summation circuit's inputs as well as finite isolation between the summation circuit's inputs. As a result, (21) shows altered gain of the inphase and delayed component. Assuming an ideal splitter, Fig. 15(b) shows that 10 dB matching and isolation ($\Gamma_1 = \Gamma_2 = 0.316, i = j \cdot 0.316$) cause up to 2.1 dB additional insertion loss, depending on the chosen delay. However, coefficients obtained from simulation of the realized circuit yield only 0.73 dB loss. It is also shown that inserting the splitter's amplitude and phase response as parameters A and B gives good accordance with the simulated results of the complete TTD circuit with lossless delay lines. The TTD circuit incorporates an active summation circuit shown in Fig. 14(a) which has higher isolation than a simple resistive power combiner

https://doi.org/10.1017/S1759078724001053 Published online by Cambridge University Press

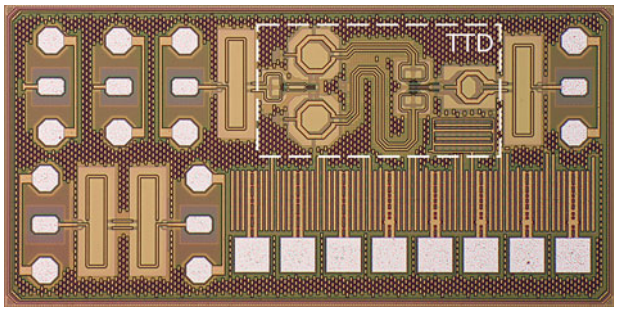

Figure 16. Micrograph of the demonstrator with fabricated D-band TTD element occupying 0.53 ×0.3 mm^2.

and allows to individually adjust the gain of the two inputs for error correction

$$G = \frac{\sqrt{1-|\Gamma_1|^2}\sqrt{1-|\Gamma_2|^2-|i|^2}}{1+\Gamma_1^2 i^2-\Gamma_1^2\Gamma_2^2}\left(A\left(1+\Gamma_1(\Gamma_2-i)\right)\right.$$
$$\left.+Be^{-j\frac{\pi}{2}}\left(1-\Gamma_1(\Gamma_2-i)\right)\right). \quad (21)$$

The demonstrator chip including calibration structures is shown in Fig. 16. It has been manufactured in IHP's SG13G2 130 nm BiCMOS technology that has an f_t/f_{max} of 350 GHz/450 GHz. The steering control and all three bias currents are individually controlled by on-chip DACs and can be optimized to compensate gain variation.

Measurement results for different bias currents of splitter, summation amplifiers, as well as the delay control byte have been obtained by on-chip measurements using a Keysight PNA-X, VDI VNAX frequency extenders, and a custom USB to serial peripheral interface adapter. Figure 17(a) shows gain, delay, and gain variation for a DC current of 6.1 mA for each amplifier. Although a gain of approximately 10 dB is achieved, gain variation suffers from asymmetry over delay setting, having the lowest gain at settings 125–190. A reduction of operating point current to 2.2 mA for the splitter and 4 mA for each summation input yields the results of Fig. 17(b) that show better symmetry but also reduced gain of 1.6 dB and a 3 dB bandwidth from 130 GHz to 156 GHz. Relative phase delay shows a tuning range of 1.63 ps and a good agreement with the simulated curves, yielding a Root mean square (RMS) delay error of 48 fs. The RMS delay error is derived from the shown measurement curves using the simulated delay, averaged over the TTD element's bandwidth, as reference. Within the bandwidth, gain differs between the different delay settings by maximally 2.8 dB and shows an RMS error of 1.0 dB. To reduce gain variation, a delay dependent biasing scheme is used. The splitter is set to 1.7 mA and the summation stages of long and short line to 3.6 mA and 2.2 mA. The currents of the summation stages are increased by a quadratic boost factor up to a maximum of 7.6 mA, respectively 4.8 mA, at delay setting 127. The results in Fig. 17(c) show a reduction of maximum gain error to 0.5 dB and an RMS gain error of 0.2 dB while gain is slightly reduced to 0 dB and the delay range is now 1.75 ps.

Table 3 gives a comparison of the uncompensated and compensated TTD element with other sub-THz TTD elements and wideband TTD elements with high delay range. In contrast to the passive implementation of switch based TTD implementations [8, 20], the presented TTD element does not have high losses but is more limited in terms of bandwidth due to the amplifiers. The employed working principle is limited to approximately 90° delay range at its highest frequency and therefore has a smaller tuning range, but it does offer high delay resolution that is only limited by the integrated 8-bit DAC, although higher linearity would be desirable that is found to be currently limited by the parasitic emitter resistance of the splitting stage's transistors and imperfect matching of the delay lines. Still, a good accordance between simulation and measurement is found resulting in an RMS delay error of 44 fs. A combination of the presented principle with a switched topology appears appealing as area requirements of [20] and gain variation of [8] seem to be further improvable without introducing phased subarrays that cause grating lobes. As better linearity and gain variation are expected with wider transistors and lower delay to signal period ratio τ/T, the presented concept is also a possible candidate for continuous and calibration free baseband TTD elements, that are currently realized using varactors [9, 12].

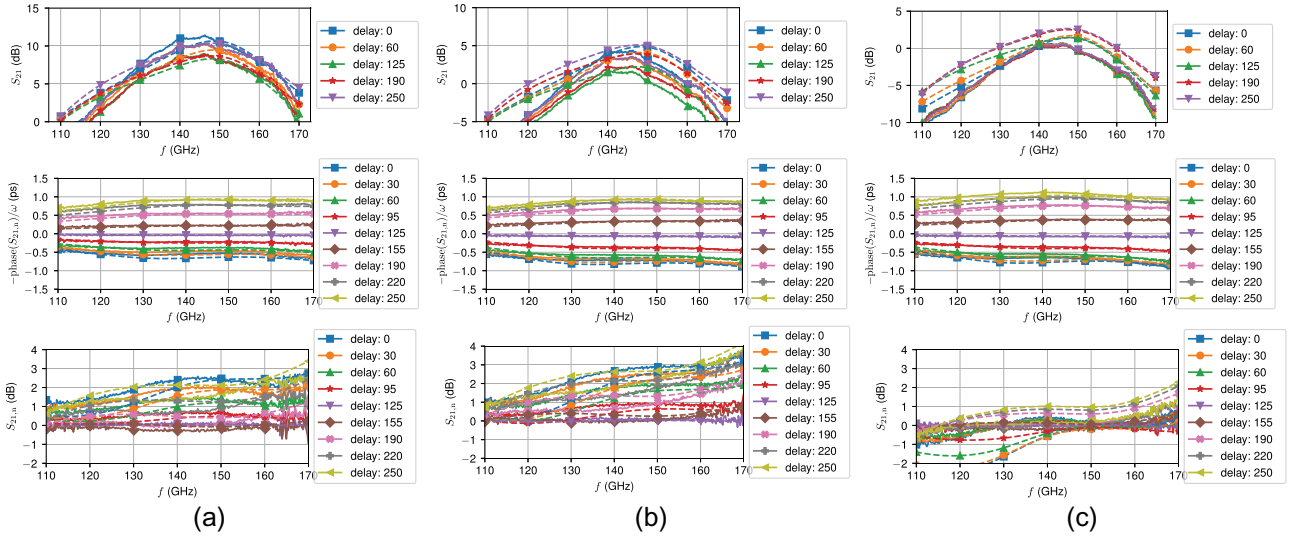

Figure 17. Measured (solid) and simulated (dashed) gain, relative delay, and relative gain of the D-band TTD element for (a) an overall constant bias current of 19.3 mA, (b) 10.9 mA, and (c) compensation of gain variation by a quadratic boost in bias current, yielding 9–15 mA current consumption.

https://doi.org/10.1017/S1759078724001053 Published online by Cambridge University Press

Table 3. Uncompensated and compensated performance of the D-band TTD element in comparison with TTD elements above 100 GHz and wideband TTD elements with high delay range.

	This, [1]	**This, [1]** comp.	**[20]**	**[8]**	**[21]**	**[22]**	**[9]**	**[10]**	**[11]**	**[12]**	**[19]**
Architecture	Delay interp.	Delay interp.	Switched TL	Switched ATL, self-switched network	Switched TL, phase shifter	Switched TL	Switched TL, tuned TL	Switched allpass, self-switched network	Switched ATL	Switched ATL, switched allpass, tuned allpass	Switched ATL
Center freq.	144 GHz	144 GHz	140 GHz	140 GHz	235 GHz	275 GHz	30 GHz	11 GHz	11 GHz	10.5 GHz	11 GHz
Absolute BW	26 GHz	26 GHz	60 GHz	60 GHz[c]	30 GHz	110 GHz	40 GHz	18 GHz	20 GHz	19 GHz	18 GHz
Delay range	1.63 ps	1.75 ps	6.64 ps	6.9 ps	1.47 ps	3.398 ps	32.8 ps	145 ps	274 ps	400 ps	508 ps
Delay resolution	cont.	cont.	0.446 ps	0.223 ps	0.39 ps, cont.	0.227 ps	4 ps, cont.	2.5 ps	34.2 ps	40 ps, 5.6 ps, cont.	4 ps
Gain (dB)	1.6	0	−21	−10.6	−8.6	−8.1	−15.5[a]	−20[c]	−20[c]	−35[c]	−3.6
Max. gain error	2.8 dB	0.5 dB	2.5 dB[c]	2 dB[c]	3 dB[b]	1.28 dB	4.6 dB[a,c]	7.3 dB[c]	9 dB	14 dB[c]	4.1 dB[c]
RMS gain error	1.0 dB	0.2 dB	1.4 dB	0.57 dB	–	0.12 dB	3 dB[a]	–	–	–	1.6 dB
RMS delay error	48 fs	44 fs	167 fs[c]	30 fs	–	90 fs	–	2.2 ps	–	–	10 ps
P_{DC} (mW)	27.2	37.5	6.2	0	4.3	0	0	0	6.2	6.0	285
Core area (mm^2)	0.159	0.159	1.166	0.04	0.22[c]	0.485[c]	0.22	5.6	1.125	4.0	3.4[c]

[a]Only over limited BW;
[b]uncompensated;
[c]extracted from graph.

Conclusion

A broad overview on the shortcomings associated with phased arrays in the context of wideband millimeter-wave array systems is given. Losses, introduced by the well-known beam squint effect, are determined by pattern simulation as well as delay differences applied to baseband signals causing ISI. Both methods give a maximum insertion loss of 5.1 dB for an exemplary eight-element D-band antenna array. Pattern simulation further shows a drastic increase in loss if the scan angle is misaligned. Timed arrays do not suffer from beam squinting and the according losses which also makes them much more tolerant to beam misalignment. However, as TTD elements are more difficult to realize than phase shifters, formation of sidelobes due to delay quantization and combination of TTD elements with phase shifters is summarized utilizing analysis methods from literature. Further, integration of delay elements with frequency conversion circuits is investigated as a measure to reduce TTD requirements, e.g. by combining baseband TTD with LO phase shifting. In a state-of-the-art overview, TTD realizations are compared to the bandwidth achieved with an ideal phased array, showing that most millimeter-wave implementations are not able to improve the available bandwidth due to a lack of bandwidth and delay range while better suitability of baseband TTD elements is observed. However, despite limited bandwidths, evaluation of sidelobe levels shows that TTD elements can be also useful to suppress sidelobes that are present in combined timed and phased arrays. Additionally, TTD resolution requirements for sufficient sidelobe suppression are compared as well as area efficiency. Subsequently, different TTD operational principles are briefly described, including switched delay elements, switch integrated delay elements, and continuous delay elements. Finally, extended content on the delay interpolation TTD principle, a system concept using this principle and a D-band TTD realization, previously published in [1], are presented. The hierarchical system concept shows the general suitability of the delay interpolation principle for beamforming in the RF and IF signal paths if its gain variation can be compensated. The description of the integrated D-band TTD element has been extended by a detailed analysis of the splitter component and reflections on the delay lines that mainly cause deviation from the ideal transfer function due to parasitic emitter resistance and imperfect matching. The TTD element achieves a continuous 1.75 ps delay range with only 0.5 dB gain variation by employing a simple gain compensation scheme. It operates at a center frequency of 144 GHz and has a bandwidth of 26 GHz. The required core area is $0.53 \times 0.3\ \text{mm}^2$.

Acknowledgements. The authors acknowledge the financial support by the Federal Ministry of Education and Research of Germany in the project "Open6GHub" (grant number: 16KISK005).

Competing interests. The author(s) declare none.

References

1. **Koch M, Probst F, Breun S and Weigel R** (2023) A continuously adjustable true time delay for D-band timed antenna arrays. 18th European Microwave Integrated Circuits Conference, Berlin, Germany.
2. **Balanis CA** (2005) *Antenna Theory: Analysis and Design*, 3rd Edn. Hoboken, NJ: Wiley.
3. **Mailloux R** (2018) *Phased Array Antenna Handbook*, 3rd Edn. Norwood, MA: Artech House.
4. **Zhang Z, Yin Y and Rebeiz GM** (2021) Intersymbol interference and equalization for large 5G phased arrays with wide scan angles. *IEEE Transactions on Microwave Theory and Techniques* **69**, 1955–1964.
5. **Mailloux R** (1984) Array grating lobes due to periodic phase, amplitude, and time delay quantization. *IEEE Transactions on Antennas and Propagation* **32**, 1364–1368.
6. **Yajima M and Hasegawa T** (2005) Beam pointing error of wideband phased array antennas with reduced true-time-delay devices. IEEE Global Telecommunications Conference, St. Louis, MO, USA.
7. **Park K and Min BW** (2021) Delay-sum group delay controller with low-loss and low-phase variation. *IEEE Transactions on Microwave Theory and Techniques* **69**, 825–832.
8. **Abbasi M and Lee W** (2024) A low-loss passive D-band phase shifter for calibration-free, precise phase control. *IEEE Journal of Solid-State Circuits* **59**, 1371–1380.
9. **Ma Q, Leenaerts D and Mahmoudi R** (2014) A 10–50 GHz true-time-delay phase shifter with max 3.9 % delay variation. IEEE Radio Frequency Integrated Circuits Symposium, Tampa, FL, USA.
10. **Willms JG, Ouacha A, de Boer L and van Vliet FE** (2000) A wideband GaAs 6-bit true-time delay MMIC employing on-chip digital drivers. 30th European Microwave Conference, Paris, France.
11. **Hu F and Mouthaan K** (2015) A 1–21 GHz, 3-bit CMOS true time delay chain with 274 ps delay for ultra-broadband phased array antennas. European Radar Conference, Paris, France.
12. **Hu F and Mouthaan K** (2015) A 1–20 GHz 400 ps true-time delay with small delay error in 0.13 μm CMOS for broadband phased array antennas. IEEE MTT-S International Microwave Symposium, Phoenix, AZ, USA.
13. **Ulusoy A, Schleicher B and Schumacher H** (2011) A tunable differential all-pass filter for UWB true time delay and phase shift applications. *IEEE Microwave and Wireless Technology Letters* **21**, 462–464.
14. **Ma Q, Leenaerts D and Mahmoudi R** (2013) A 12 ps true-time-delay phase shifter with 6.6 % delay variation at 20–40 GHz. IEEE Radio Frequency Integrated Circuits Symposium, Seattle, WA, USA.
15. **Woods WH, Valdes-Garcia A, Ding H and Rascoe J** (2013) CMOS millimeter wave phase shifter based on tunable transmission lines. IEEE Custom Integrated Circuits Conference, San Jose, CA, USA.
16. **Garakoui SK, Klumperink EAM, Nauta B and van Vliet FE** (2015) Compact cascadable g^m-C all-pass true time delay cell with reduced delay variation over frequency. *IEEE Journal of Solid-State Circuits* **50**, 693–703.
17. **Shin DH, Yom IB and Kim DW** (2017) 4–20 GHz GaAs true-time delay amplifier MMIC. *IEEE Microwave and Wireless Technology Letters* **27**, 1119–1121.
18. **Kim KJ, Hong Kang J, Hwang JH and Ahn KH** (2018) Hybrid beamforming architecture and wide bandwidth true-time delay for future high speed communications 5G and beyond 5G beamforming system. 3rd International Conference on Integrated Circuits and Microsystems, Shanghai, China.
19. **Cho MK, Song I and Cressler JD** (2018) A true time delay-based SiGe bi-directional T/R chipset for large-scale wideband timed array antennas. IEEE Radio Frequency Integrated Circuits Symposium, Philadelphia, PA, USA.
20. **Karakuzulu A, Eissa MH, Kissinger D and Malignaggi A** (2020) Broadband 110–170 GHz true time delay circuit in a 130 nm SiGe BiCMOS technology. IEEE MTT-S International Microwave Symposium, Los Angeles, CA, USA.
21. **Steinweg L, Carta C and Ellinger F** (2022) A hybrid true-time and phase-delayed approach for millimeter-wave beam steering. *IEEE Transactions on Microwave Theory and Techniques* **70**, 4318–4327.
22. **Maurette-Blasini C, Kuliabin K, Chartier S and Quay R** (2022) An H-band mHEMT-based millimeter-wave true-time delay MMIC. 14th German Microwave Conference, Ulm, Germany.
23. **Govind B, Tapen T and Apsel A** (2024) Ultra-compact quasi-true time delay for boosting wireless channel capacity. *Nature* **627**, 88–94.
24. **Garakoui SK, Klumperink EAM, Nauta B and van Vliet FE** (2011) Phased-array antenna beam squinting related to frequency dependency of delay circuits. 41st European Microwave Conference, Manchester, UK.
25. **Zolkov E, Weiss R, Madjar A and Cohen E** (2021) A low power consumption 65 nm CMOS true time delay N-path circuit achieving 2 ps delay resolution. 15th European Microwave Integrated Circuits Conference, Utrecht, Netherlands.

https://doi.org/10.1017/S1759078724001053 Published online by Cambridge University Press

26. **Lee W and Valdes-Garcia A** (2019) Continuous true-time delay phase shifter using distributed inductive and capacitive miller effect. *IEEE Transactions on Microwave Theory and Techniques* **67**, 3053–3063.
27. **Shen J, Zhang Y, Yang L, He L, Guo Y and Gao H** (2021) Wideband digitally controlled true time delay for beamforming in a 40 nm CMOS technology. IEEE International Symposium on Circuits and Systems, Daegu, Korea.

Manuel Koch received the M.Sc. degree in electrical engineering, electronics and information technology from the Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Erlangen, Germany, in 2020. He then joined the FAU as a Research Associate where he is currently working toward the Ph.D. degree. His research interests include BiCMOS millimeter-wave integrated circuits for 6G communication in D-Band.

Stefan Schönhärl holds an M.Sc. degree in electrical engineering from the Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Erlangen, Germany, attained in 2023. His master's thesis delved into D-band phase shifters. Currently, Stefan is a Research Associate with the FAU. In his pursuit of a Ph.D. degree, he primarily works on the research of integrated hardware and system aspects for D-Band beamforming.

Sascha Breun received the M.Sc. degree in electrical engineering from the Friedrich-Alexander-Universität Erlangen-Nürnberg, Erlangen Germany, in 2018. For his master's thesis, he joined Infineon Technologies, Munich, to work on the modeling of integrated inductors and transformers for millimeter-wave (mm-wave) radar circuits. He is currently a Research Associate with the Friedrich-Alexander-Universität Erlangen-Nürnberg.

Georg Fischer received the degree in electrical engineering from RWTH Aachen University, Aachen, Germany, in 1992, and the Dipl.-Ing. (TH) degree in electrical engineering and the Dr.-Ing. degree (summa cum laude) from the University of Paderborn, Paderborn, Germany, in 1992 and 1997, respectively. From 1993 to 1996, he was a Research Assistant with the University of Paderborn. In 1996, he joined Bell Labs, Research of Lucent Technologies, Germany, focusing on base-station RF technology. He was promoted to a Bell Labs Distinguished Member of Technical Staff (DMTS), in 2000, and a Bell Labs Consulting Member of Technical Staff (CMTS), in 2001. In 2007, he was nominated for Bell Labs Fellow. In 2008, he was appointed as a Full Professor of electronics engineering with Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Erlangen, Germany. Prof. Fischer is a member of EuMA and VDE and named inventor on more than 50 patents.

Robert Weigel was a Professor of RF Circuits and Systems with the Munich University of Technology, Munich, Germany from 1994 to 1996. From 1996 to 2002, he was a Full Professor and the Director of the Institute for Communications and Information Engineering, University of Linz, Linz, Austria. In Linz, in August 1999, he co-founded the company DICE, meanwhile split into an Infineon Technologies Company and an Apple Company [in between an Intel Company (DMCE)] which are devoted to the design of integrated circuits and systems. From 2002 to 2024, he has been a Full Professor and the Director of the Institute for Electronics Engineering, now part of the Institute for Smart Electronics and Systems, Friedrich-Alexander-Universität Erlangen-Nürnberg, Erlangen, Germany. In 2012, he co-founded the company eesy-ic, devoted to RF and mixed-signal circuits. He has been engaged in research and development of microwave theory and techniques, electronic circuits and systems, and communication and sensing systems.

https://doi.org/10.1017/S1759078724001053 Published online by Cambridge University Press