

## Research Paper

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# Bare die connections via aerosol jet technology for millimeter wave applications

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## Abstract

This paper presents a comparison of chip connections using aerosol jet (AJ) and bond technology on low-cost printed circuit board (PCB) substrates. First, the behavior of the used gap filler material and the used silver ink for AJ technology on PCBs are characterized. In addition to comparing the radio frequency (RF) performance (DC to 67 GHz) of the two technologies, the mechanical stability is also compared. While the AJ technology transitions score above all for their RF performance and the lower requirements (surface finish, pad size, and adhesion) on the PCB, the bonding technology has clear advantages, especially with a different coefficient of thermal expansion values of the substrates to be connected. Finally, the measurement results of a complete package are shown, whereby the chip connection is realized once by means of AJ and once by bonding wires.

## Introduction

The increasing structural accuracy of conventionally manufactured printed circuit boards (PCBs) with wet-chemical etching processes allows more and more millimeter wave applications to be realized directly on circuit boards. What was previously only achieved directly on the semiconductor or on ceramic chip carriers (e.g. couplers or filters) can now be inexpensively and individually integrated into the PCB. By packaging with organic substrates, radio frequency (RF) chips for applications up to 67 GHz can be integrated in standard PCB substrates [1]. In addition to the PCB connector, the signal path on the PCB and the PCB-package transition, the connection of the chip itself pushes its limit. Broadband applications (e.g. for signal generators with 1.00 mm coaxial system) require transitions with low return loss up to 110 GHz. Here, the conventional wire bonding technology (Fig. 1) reaches its limits. By differential signal routing, a broadband transition between package and chip can be expanded up to 67 GHz [2]. Narrowband transitions in this frequency range are possible. Broadband single ended transitions generate much earlier unacceptable reflections. Additive built transitions using aerosol jet printing technology (AJT) have a significantly lower inductive character and, therefore, should allow transitions with lower reflection coefficients.

## Aerosol jet technology

Using the aerosol jet (AJ) technology, a variety of materials can be deposited selectively and maskless. In the field of PCB technology, the additive method has distinct advantages with respect to the achievable structure accuracy in contrast to the traditional subtractive wet chemical etching process. Here, structures can be realized down to 10 µm line width and 10 µm space. Since the method works contactless, it can create structures on almost any surface or shape. Compared with inkjet technologies (IJT), AJT allows narrower and thinner lines.

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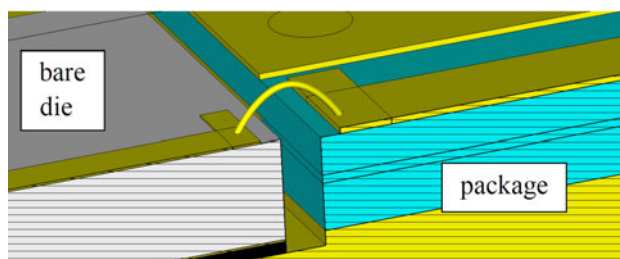


Fig. 1. Bonded package – chip transition (schematic, cross-section).

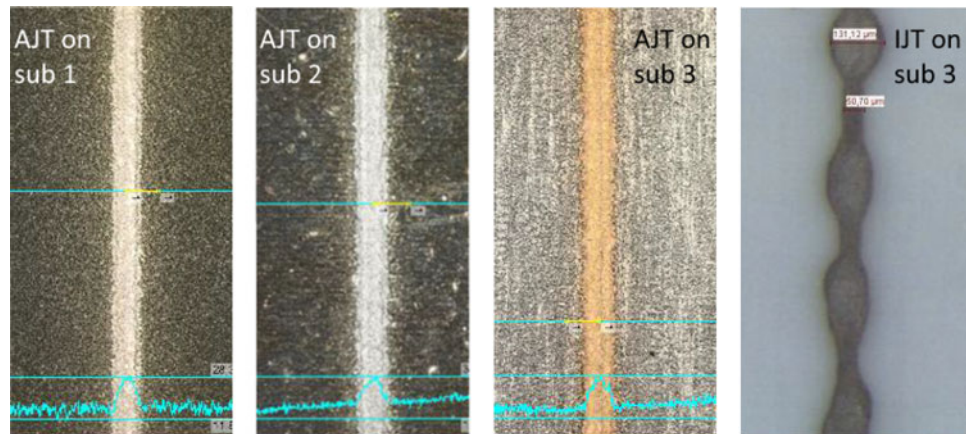


Fig. 2. AJT and IJT printed 50  $\mu\text{m}$  lines on different RF PCB substrates.

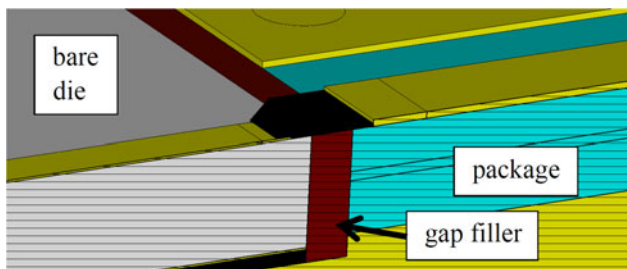


Fig. 3. Printed package – chip transition (schematic, cross-section).

PCBs for RF applications can be made of different PCB materials. In principle, a distinction is made between three groups: FR-4 materials with ceramic fillers (substrate 1 in Fig. 2), Polytetrafluoroethylene-based materials (substrate 2 in Fig. 2) and liquid crystal polymer materials (substrate 3 in Fig. 2). These materials differ in their surface properties partly clear. Unlike IJT, however, AJ technology has the advantage that it adheres to all three material groups (Fig. 2) without having to change the manufacturing parameters significantly. In addition, the layer thickness and conductor width can be set much more precisely than with inkjet, because the proportion of volatile components in AJ inks is significantly lower than in inkjet inks. This is especially important for multiple prints.

Furthermore, the morphology is independent of the printing direction [3]. The use of AJT to generate lines of silver ink is well-documented [4, 5]. Thus, on the one hand, the RF characterization of AJ printed lines is published [6–10] and on the other hand, the AJT has been used to connect chips [11]. Nevertheless, to the authors' knowledge, there is still no public research to connect chips to circuit boards (Fig. 3) for millimeter wave applications.

For printing chip transitions, an AJ Printer with pneumatic atomizer (fine feature deposition head with heater and shutter;  $\pm 6 \mu\text{m}$  accuracy motion system; feature size to  $10 \mu\text{m}$ ) provided by Fraunhofer IKTS was employed. The ink applied is a commercially available silver nanoparticle ink (Paru PG-007) with a silver content of 70% per weight and a surface tension of  $50 \text{ mN/m}$ . After depositing, the nanoparticle ink requires a thermal post-treatment to enable the solvent to evaporate and to achieve good electrical conductivity by initializing sintering of the

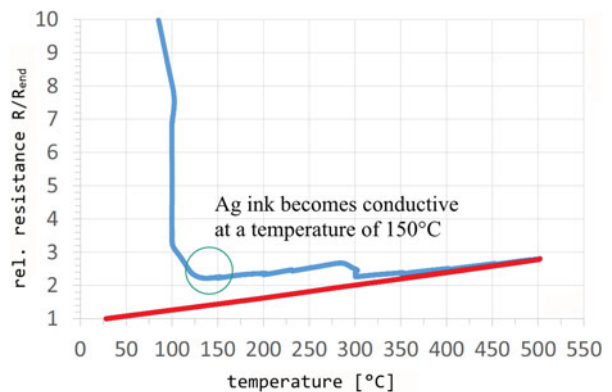


Fig. 4. Achievable electrical resistance versus sintering temperature of Ag Ink.

particles. Generally, it can be said, the higher the sintering temperature, the better the electrical conductivity. For usual PCBs it is important that the temperature is not above  $170^\circ\text{C}$ . Higher sintering temperatures for best reliability, e.g.  $600^\circ\text{C}$  and above [8], would destroy the PCB substrates. Figure 4 shows the achievable relative electrical resistance as a function of the sintering temperature of the analyzed silver ink and the relative resistance of  $R_{\text{end}}$  depending on temperature (cooling curve). The measurement results were obtained experimentally by measuring the resistance of a printed line during the sintering and cooling phase. Since the ink already reaches its 2–3 times minimum resistance ( $R_{\text{end}}$ ) value at a temperature of  $150^\circ\text{C}$ , the ink is very suitable for use on organic PCBs.  $R_{\text{end}}$  is the resistance of the silver ink at room temperature when sintering with a temperature of  $500^\circ\text{C}$ . The temperature coefficient of resistance (TCR) of the AJ silver ink ( $3.77 \times 10^3 \text{ 1/K}$ ) is nearly the same as the TCR of a pure silver bulk ( $3.8 \times 10^3 \text{ 1/K}$ ). The TCR was determined by the cooling curve of the resistance. By comparison, inkjet inks have a twice as high electrical resistance due to their lower silver content (<50% compared with AJ inks).

Nearly as important and challenging as the conductive chip connection is the filling of the gap between chip and package with a nonconductive material. Due to dimensional fabrication tolerances of the bare die and primarily the PCB, the gap between bare die can have between 50 and 200% of its nominal value. In

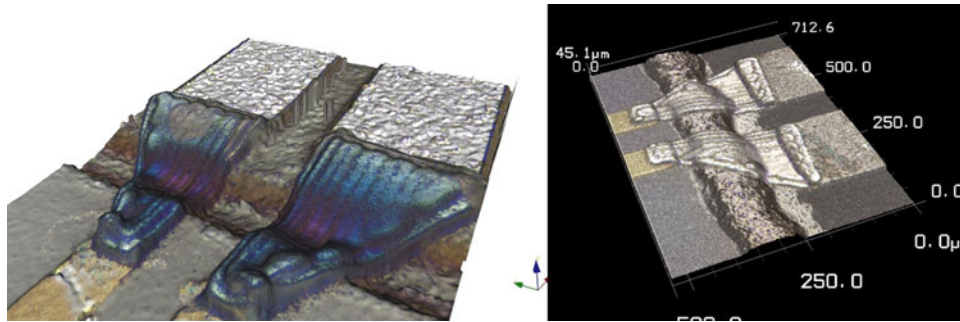


Fig. 5. Incorrect (left) and correct (right) filled gap.

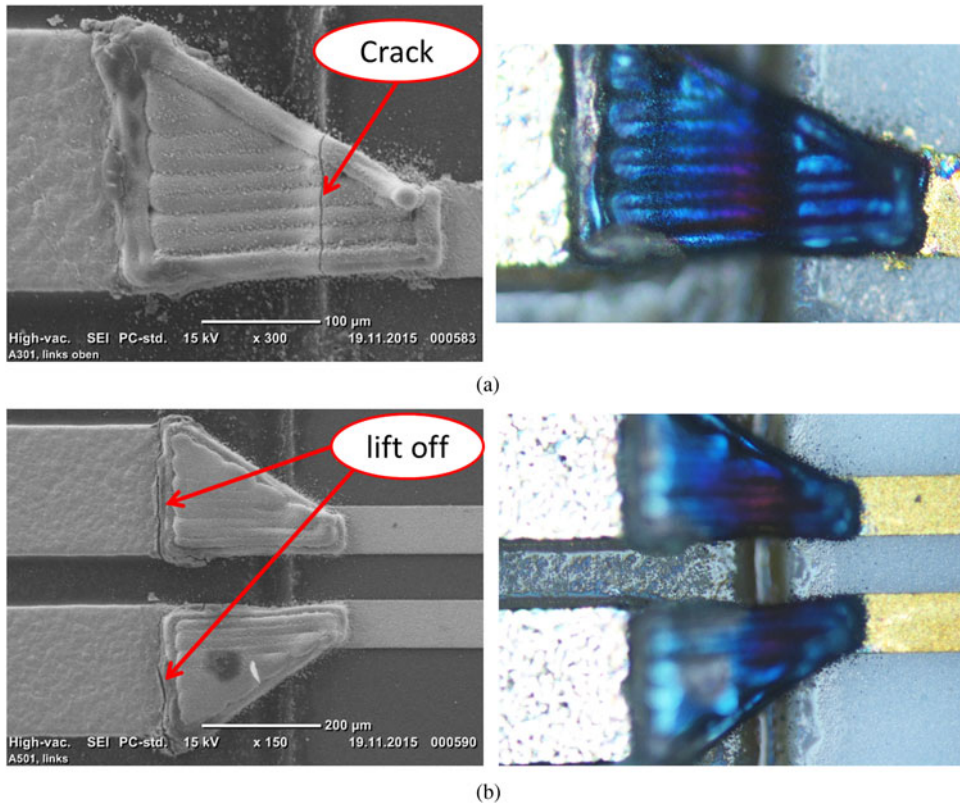


Fig. 6. Failure images of AJ printed lines caused by wrong gap filling.

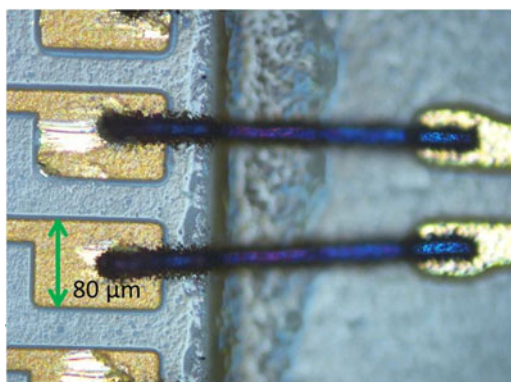
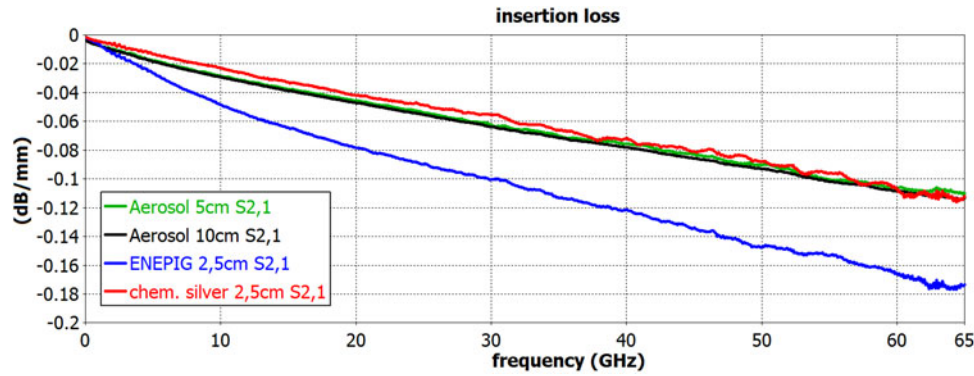


Fig. 7. Common wire Bond Pads connected via AJ.

our case, the gap has a nominal width of 100  $\mu\text{m}$  and a depth of 290  $\mu\text{m}$  (height of bare die, metallization, and conductive adhesive). It is of particular importance that the gap is filled in a precisely defined way. The gap filler material must neither overflow nor fill the gap only partially. Therefore, a camera-supported individual filling of each gap is applied. The filler used was the commercially available Epotek H70-175 adhesive. With a particle size of 20  $\mu\text{m}$  it is easy to dose and still liquid enough to evenly fill the gap.

**Mechanical stability in comparison with bond technology**

An important point is first how the gap between bare die and PCB is filled. Optimum mechanical stability is achieved when the gap



**Fig. 8.** Insertion loss of aerosol lines compared with common PCB lines (substrate 1 of Fig. 2: Panasonic Megtron 6<sup>®</sup>, substrate thickness = 100  $\mu\text{m}$ , DK = 3.36 @ 40 GHz, DF = 0.01 @ 40 GHz [2]).

is filled slightly over-inflated so that the substrate for the ink only has flat or obtuse angles (Fig. 5). If there are right or even acute angles, the printed AJ lines may lift off (due to different thermal expansion coefficients of PCB, gap filler, and bare die) or form cracks. Both lead to discontinuities on the transmission lines, which make signal transmission impossible.

Cracks are particularly critical as they are extremely hard to see visually by optical microscopes (Fig. 6, right). Only a technology like scanning electron microscopy reveals a crack or lift off in the AJ line (Fig. 6, left).

In contrast to bonding wires, however, the surface finish of the contact points to be connected (PCB and bare die) can be selected almost arbitrarily. Thus, for example, a cheap and highly conductive silver surface can be used on the PCB substrate instead of special bondable metallization like ENEPIG<sup>®</sup>.

It is only important that the surface is not too smooth (roughness  $>0.2 \mu\text{m}$ ) and that the coefficient of thermal expansion (CTE) mismatch of the materials used (bare die, gap filler, PCB) is not too high. Moreover, there is no restriction in bond pad size. Common bond pads should not have a size below  $80 \mu\text{m} \times 80 \mu\text{m}$ , otherwise the pad can be destroyed during the bond process. AJ pads can have a much smaller size (Fig. 7) because there is no mechanical stress during AJ process.

In addition, it is important that the gap filling material is fully cured before the AJ print so that no subsequent stress is built upon the silver ink. The last point to keep in mind is the number of deposited ink layers for a connection. Depositing too few layers, the conductance of the connection reduces too much. If one applies too many, the ink cannot compensate the CTE mismatch between bare die and PCB any more leading to the failures shown in Fig. 6. For the materials used here, the most stable transitions were created with three print passes and a final ink thickness of 16–17  $\mu\text{m}$ . In this case, the horizontal tolerances are smaller than 3  $\mu\text{m}$ . The AJ Printer can print lines with a velocity of 4–6 mm/s. This means a printing time of nearly 15 s/transition with one printing nozzle, which is significantly higher than conventional well-optimized wire bonders.

### Electrical RF characterization of gap filler material and silver ink

For the most mechanically stable configuration (three print passes, 150°C sintering temperature for 1 h) a bulk resistance of 3.5  $\text{m}\Omega/\text{sq}$  was achieved. This is almost 4 times as high as that

of a comparable copper line (0.88  $\text{m}\Omega/\text{sq}$ ). However, the lines can be realized very smoothly and with an accuracy of  $\pm 3 \mu\text{m}$ , which makes AJ ideal for impedance critical applications. Conventional wet-chemically etched copper lines can currently only be realized with an accuracy of  $\pm 5 \mu\text{m}$  with high-end technology [12].

Looking at the RF performance of AJ printed silver ink lines, they achieve similar transmission loss values as silver coated copper wires (Fig. 8). The reason is that surface roughness and dielectric losses dominate the losses in the GHz range and the reduced bulk resistance has virtually no influence. It is also striking that the AJ lines thus also have a significantly lower insertion loss than lines with bondable surfaces (e.g. ENEPIG). ENEPIG [13] is an end surface with a relatively thick nickel layer (4–7  $\mu\text{m}$ ), which is required for gold wire bonding. The relative hard nickel allows the bond wires to form a robust connection to the copper line on the PCB. Silver lines on the PCB are not suitable for bonding applications because they are too soft and do not bond sturdily enough to the bond wires. Tests, that simulate soldering procedures in reflow workstations with temperatures up to 268°C (three cycles á 6.33 min) did not change the RF performance of the AJ lines. A measurement of samples stored for 12 months in room atmosphere has shown that the insertion loss of the AJ lines without passivation has deteriorated only by 0.005 dB/mm (@40 GHz).

To determine the electrical properties of the gap filler material, gaps were lasered into the PCB with well-known electrical properties (same material as used in Fig. 8). These were filled with the gap filler material and afterward overprinted with AJ (Fig. 9). The impedance steps of different gap widths were then analyzed with a R&S ZVA 67 GHz network analyzer in the time domain. For the determination of the electrical properties, the largest investigated gap with 500  $\mu\text{m}$  is most suitable since it requires the lowest spatial resolution. Since the impedance steps at a gap width of 200  $\mu\text{m}$  are not very different from the impedance of the gap width of 500  $\mu\text{m}$ , it can be assumed that the spatial resolution is high enough. To obtain an impedance of 50  $\Omega$  with the here printed line width of 215  $\mu\text{m}$ , the necessary material parameters of the filling material can be determined by simulation (Fig. 9, bottom). Simulations with a dielectric constant (DK) of 4.2 and a dissipation factor (DF) of 0.016 for the gap filling material lead to best matching to the measurement results. The datasheet gives a value for DK of 4.72 (@ 1 kHz) and no value for DF.

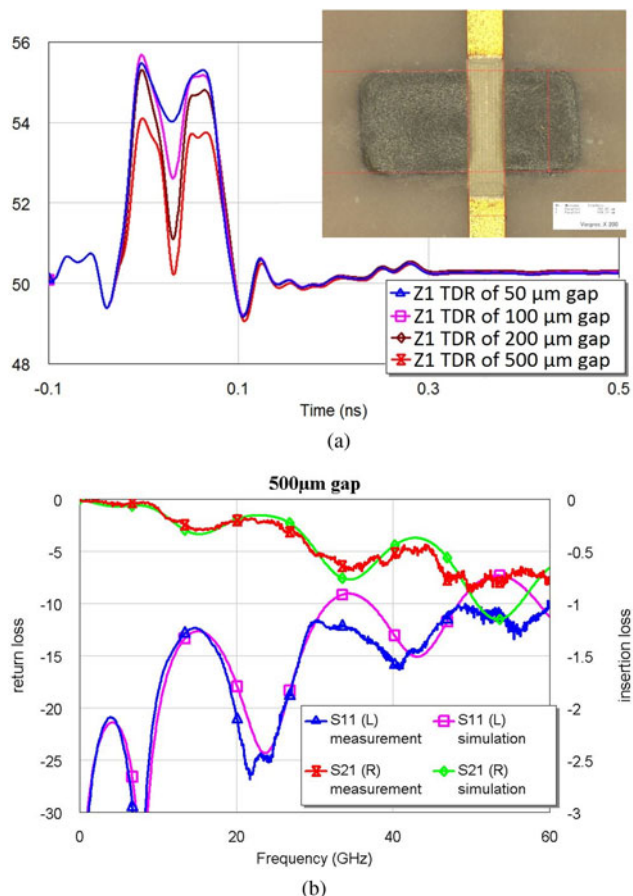


Fig. 9. Impedance steps of different gaps printed by AJ (top) and S-Parameter comparison of 500 μm gap (simulation and measurement, bottom).

### Measured performance of AJ connection

As chip carriers, the packages well-characterized in [2] were used. The fabricated broadband differential structures allow an analysis of the aerosol transition from DC to 67 GHz. The measurement setup and the deembedding procedures used are identical to those in [2].

Figure 10 shows the comparison of an AJ and a bond transition. The transition contains one connection from baseboard to package and from package to chip. As mentioned in [2] the return loss is dominated by the transition from baseboard to package (which is still the same in both cases). The more important difference of both transition types can be seen in insertion loss. Because AJT allows silver as surface finish at the package, the insertion loss can be reduced by 0.56 dB (@40 GHz). This means a reduction of power losses of 6% absolute per transition. Moreover silver is cheaper than gold as surface finish.

Time-domain reflectometer (TDR) measurements (Fig. 11) allow to review the quality of the designed and produced packages and transitions in detail. It shows the impedance of the whole measurement path between the coaxial calibrated connectors of the VNA (frequency range from 67 MHz to 67 GHz). In comparison with the bond transition, which is matched very well to the desired 100 Ω, the impedance of the AJ transitions is too high. This may be the main reason, why the return loss of the AJ package is not as good as the return loss of the bond package in Fig. 10. However, considering that the AJ junction

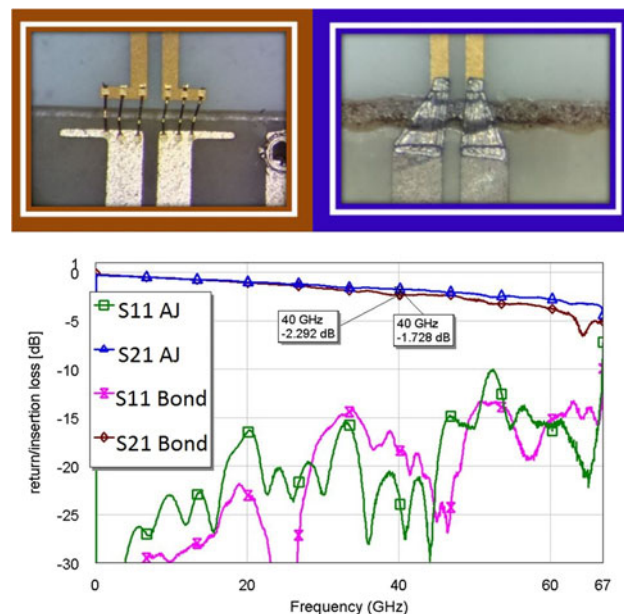


Fig. 10. Comparison of deembedded baseboard with chip transition.

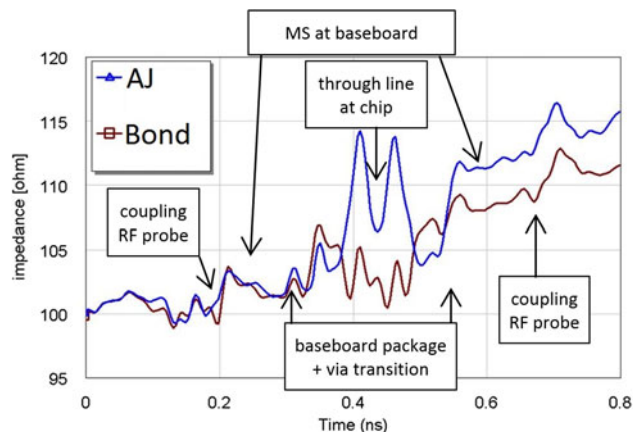


Fig. 11. TDR measurement of differential 0.65 mm BGA incl. baseboard and RF probes (measured with R&S ZVA 67).

has no compensation structures on both sides (the chip and the package, Fig. 10 top), the performance is very good. The bond transition would have been significantly worse without compensation.

### Conclusion

Currently, well-established bonding technologies for interconnections are mechanically very flexible and can bridge large distances (even over other components) especially at lower frequencies. Furthermore, the two connection points may even have materials with significantly different coefficients of thermal expansion. However, it must be ensured that the surface finishes are bondable. Especially in the millimeter wave frequency range, AJ technology offers great advantages as compared with bond wires as, in principle, any two conductive surfaces can be interconnected. It has been shown, that this leads to a significant reduction in

insertion loss. In addition, the line impedance of the interconnect can be designed as required, enabling low-loss, low-reflection broadband transitions up to the three-digit GHz range.

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