## **Industrial Applications of Electron Microscopy: A Shared Laboratory Perspective**

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New technologies and industries are emerging in recent years, for example facial recognition, autonomous driving, virtual reality, 5G communication etc. For investors, these concepts bring investment opportunities; for processing engineers, these fascinating technologies typically resonate with FinFET, VCSEL, III/V compound semiconductors; while for electron microscopists, these indicate hetero-epitaxy, cubic and hexagonal lattices, and associated failures in devices that often have complicated 3D structures.

Electron tomography [1] can provide rich information in 3D, but conventional 2D projection of a planar TEM lamella prepared by FIB is still the preferred approach in the industry. Recent development of FIB technology enables high-precision TEM sample preparation of 3D logic and memory devices. For example, in order to avoid artifact, a gate cut lamella (y-z plane) for a FinFET sketched in Fig.1(a) should be thinner than the gate length  $L_{Gate}$ . Shown in Fig.1(b) is a HAADF image of a gate cut from a 22nm generation 3D FinFET device with  $L_{Gate}$ ~30nm. For high- $\kappa$ /metal gate engineering, it is critical to know the composition of individual layers, which can be mapped with STEM/EELS spectrum imaging. Fig.1(c) and (d) show the blended EELS maps of several elements. A proper image blending mode [2] needs to be implemented to effectively present the maps to non-expert end users. 3D NAND in a solid-state drive also has similar, if not larger, challenge for TEM sample preparation. Shown in Fig.1(e) is a conventional TEM image of one memory cell. EELS analysis is found to be effective for this type of devices [3].

Electron microscopy techniques such as ECCI [4], SEM-CL [5], EBIC [6], and STEM are useful to characterize the density and types of defects in crystalline materials on a variety of length scales and spatial resolutions. Fig.2 shows examples of three techniques for locating and deriving defect densities in GaN epitaxial films. For discrete or failed devices, locating specific electrically active defects causing degradation in performance is a critical need to determining root cause. Fig.3 shows how SEM-EBIC combined with precise cross-sectional STEM analysis is utilized on a failing VCSEL to locate and target two distinct electrically active defects. Examination of the resulting cross-section shows that root cause of failure is due to excessive strain at the aperture edges leading to dislocation formation and eventual failure of the device [7]. In many instances, a combination of microscopy techniques is required to reach a fundamental understanding of the engineering problem at hand, often with urgency in real life.

References:

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**Figure 1.** (a) Structure of a FinFET device, (b) atomic-resolution HAADF image of the high- $\kappa$ /metal gate structure, (c) blended EELS map of C, N, O, W, and Si on the fin, (d) blended EELS map of Hf, Ta, Al, Ti, W, and Si on the fin, and (e) TEM image of a memory cell from a 3D-NAND solid-state drive.



**Figure 2.** Three different microscopy techniques for assessing crystal defect (dislocation) densities and typing (edge, mixed, or screw) of GaN epitaxial films. (a) Electron Channeling Contrast Imaging (ECCI), (b) Scanning Electron Microscopy Cathodoluminescence (SEM-CL), and (c) STEM.



**Figure 3.** Plan-view SEM-EBIC is utilized to locate electrically active defects at the surface of a VCSEL. Using the dark spots from the EBIC data, we can precisely target the defects by FIB for STEM Cross-Sectional analysis. XS-STEM results show there are dislocations emanating from the aperture layer edges towards the surface and into the MQW killing the device.