

Toward Automated S/TEM Metrology of Advanced CMOS Devices: Journey to Obtain a Precise and Accurate Measurement

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With the advancement of Complementary Metal Oxide Semiconductor (CMOS) development, current CD metrology faces significant challenges from shrinking critical dimensions (CD) and 3D device structures.^[1] Critical Dimension Scanning Electron Microscopy (CD-SEM) suffers from poor spatial resolution and is not applicable for sub-surface measurements. Alternatively, Scatterometry relies heavily on measurements from reference structures (which are not always available) for an accurate modeling and is performed on specific array macros rather than the real devices under test.

Transmission electron microscopy and scanning transmission electron microscopy (S/TEM) provide angstrom-level spatial resolution with a high precision, while using the silicon lattice as an internal reference for calibration. Both merits make S/TEM a great candidate for metrology. Equipped with the recipe-driven imaging, chemical analysis and CD measurements, automated S/TEM metrology becomes a practical solution. Before it becomes a metrology tool, understanding the factors that can affect the precision and accuracy of this recipe-driven S/TEM system are vital. This paper describes our journey to obtain precise and accurate measurements by automated S/TEM.

A number of factors are studied, such as imaging modes, electron beam damage, image size, dwell time/pixel, lamella tilt and camera length (Table 1). Three test structures, such as vendor's standard lamella, CMOS gates and CMOS Fins are used (Figure 1). They are composed of typical materials (i.e. Si, oxides, nitrides, low-K dielectrics and high Z materials) that are used in the semiconductor industry. Statistically meaningful results were obtained by imaging test structure under one condition with at least 10 repetitions. Pooled variance (PV) is used to estimate the variance of measurements from different structures. Figure 2 shows HAADF-STEM which, as compared to BF-TEM, gives a lower pooled variance which is an indication of a higher precision measurement. Electron beam damage on dielectrics can be clearly seen in Figure 3(a), which caused a CD increase. This damage can be alleviated by reducing probe current (Figure 3(b)) or by lowering operating voltage. Figure 4 shows that the optimum combination of image size and dwell time/pixel needs to be implemented in order to meet measurement uncertainty requirement (i.e. $3\sigma < 1\%$). CMOS devices are built along the [110] direction of Si, and CD measurements are usually made along [110]; if the lamella is not aligned closely to this direction, inaccurate measurements can be produced as shown in Figure 5. The Si lattice provides an internal reference to calibrate S/TEM images in order to attain high accuracy. These findings lay the groundwork for achieving a precise and accurate measurement in automated CD-S/TEM [2].

References:

[1] B.L. Thiel *et al*, Conference Proceedings, **1395(1)** (2011), p. 298.

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Table 1. Typical parameters used in the design of experiments.

Imaging mode	Operating voltage (kV)	Probe current	Image size	Dwell time (us)	Lamella tilt (°)	Camera length (mm)	Image contrast
BF-TEM	80	--	512	--	0	45	--
HAADF-STEM	120	-	1024	-	0.5	73	-
	200	+	2048	+	1	115	+
		++	4096	++	2	185	++

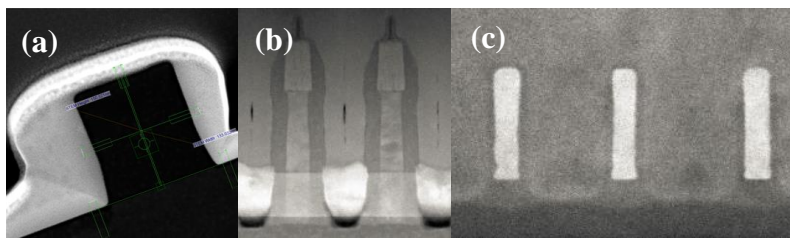


Figure 1. HAADF-STEM micrograph of (a) vendor's standard lamella, (b) CMOS gates and (c) CMOS Fins.

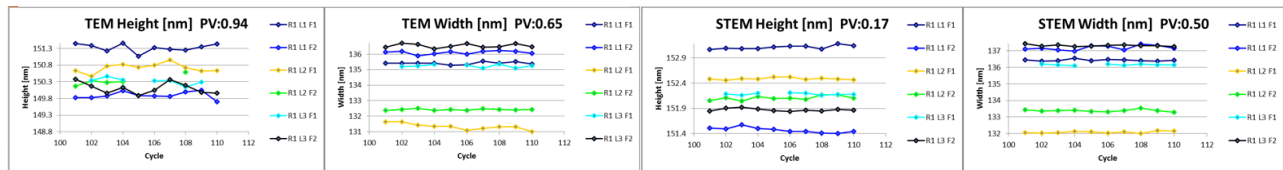


Figure 2. Pooled variances calculated from the measurements of structure in Fig.1(a).

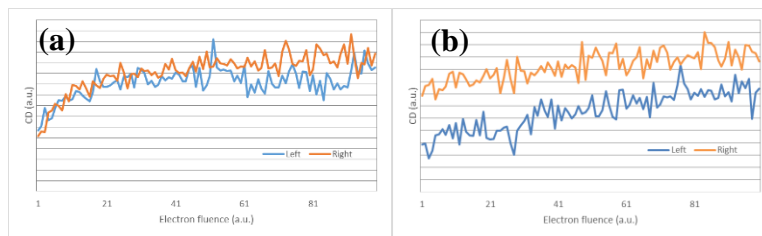


Figure 3. CDs of dielectrics in Fig.1(b) as a function of electron fluence:- (a) high probe current and (b) low probe current.

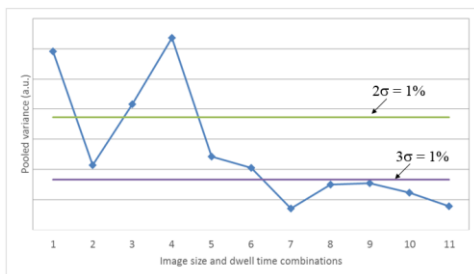


Figure 4. Pooled variances calculated from the measurements of Fig. 1(c) taken at different combinations of image size and dwell time.

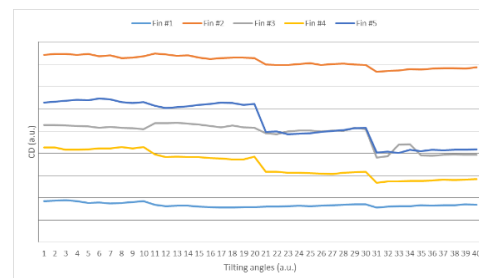


Figure 5. CDs of Fig.1(c) as a function of tilting angles.