

## **Beware of Artifacts When Characterizing Nanometer Device Features Smaller than a TEM Lamella Thickness in Semiconductor Wafer-foundries**

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With continuous shrinkage of semiconductor transistor nodes, transmission electron microscopy (TEM) analysis has become complex, more challenging, and requires knowledge/experience for correct interpretation of results. Since a TEM lamella machined by a focused ion beam (FIB) usually has a thickness around 50~150nm, there is always a chance that area of interests (AOI) are usually thinner than a TEM lamella in the case of 20nm, 14nm technology nodes and beyond [1~3]. This inevitably introduces certain artifacts due to overlapping of various portions of the device onto the final TEM images, the so-called “projection effect”, since no matter how thin, the TEM foil still has a thickness, physically. Additionally, device features are also becoming more and more complex with the advent of 3D-FinFET. Convolved together, these aforementioned factors lead the TEM interpretations less and less straightforward by inexperienced customers who are not TEM professionals but put requests and rely on the TEM analyses for process changes at wafer-foundries. Seeing always believing is the human nature to assume. Unfortunately not necessarily always true under TEM, if with the projection effect. Therefore, another big task for TEM analysts at wafer-foundries is to educate and ensure TEM customers fully understand what the Analytical TEM results imply, in addition to get the most out of what TEM instruments have to offer in a timely fashion. Working as a team with frequent and close interactions between TEM analysts and internal customers is a big virtue from design of experiments on sample-preparation to eventually interpret the TEM results correctly so that meaningful feedback can quickly be applied to on-going yield enhancement at wafer-foundries.

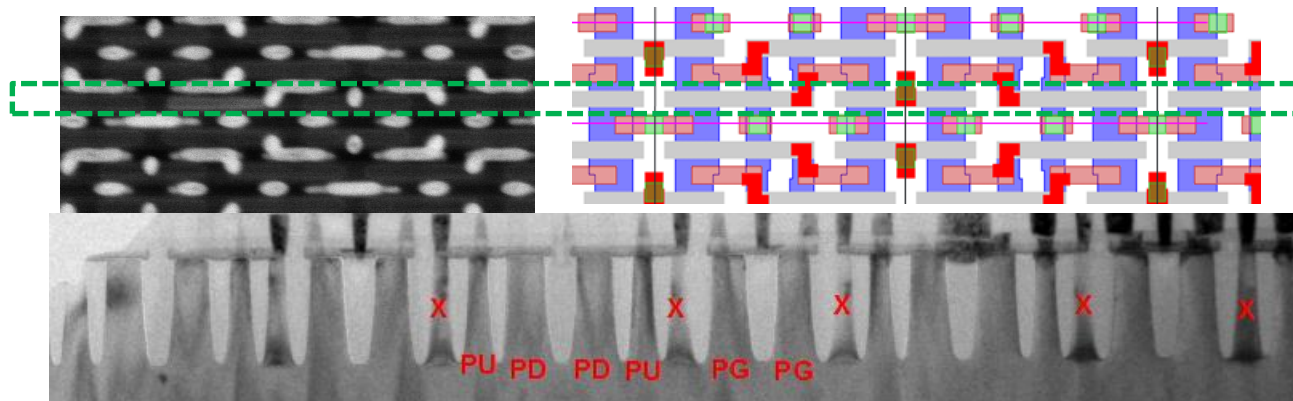
Presented here are few common examples of artifacts noticed while characterizing SRAM transistors of 20nm or below by TEM, that the process and integration teams need to be aware of. Full understanding of such geometrical artifacts associated with variations in TEM lamella thickness and exact locations where TEM foils being extracted, will significantly reduce unnecessary TEM requests and minimize potential follow-ups. This in turn translates the efforts in coaching customers for productivity improvement. These challenges are applicable not only to semiconductor and nanotechnology, but also a good educational topic to general scientific and engineering communities. Figures-1 illustrated that a TEM lamella could typically be extracted in different locations and thickness. The SEM image is a top-down view of SRAM device and corresponding cross-sectional TEM image displaying how artefacts diminishing with progressively thinned TEM lamella. Figures-2 demonstrated how “projection effect” of SiGe epi in a PFET in SRAM diminishing with reduction of TEM lamella thickness until critical dimensions measured confidently. Figures-3 show that the seemingly extra species under PC gate stacks near edge of a PFET bank. These were actually a projection effect due to undulation at the long channel PC bottom in a thick TEM sample and not foreign materials as verified by XEDS elemental mapping and linescan.

References:

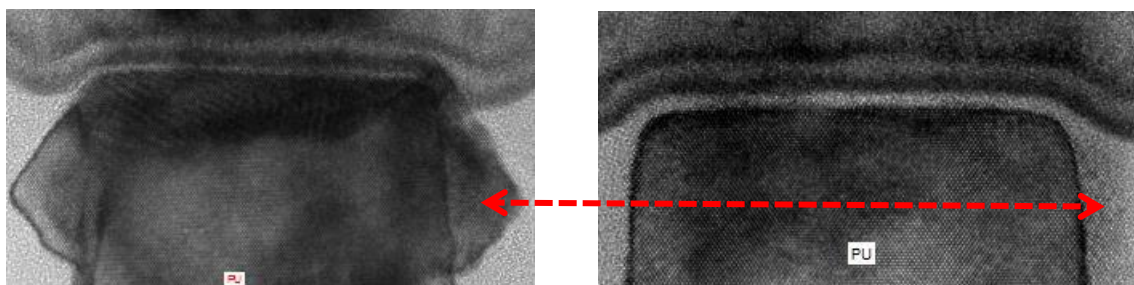
[1] W. Zhao, *et al.*, *Microscopy & Microanalysis*, Vol. 19 (Supplement 2), (2013), pp.902~903.

[2] W. Zhao, *et al.*, *Proc. 38<sup>th</sup> International Symposium for Testing and Failure Analysis*, (2012), pp. 347~355.

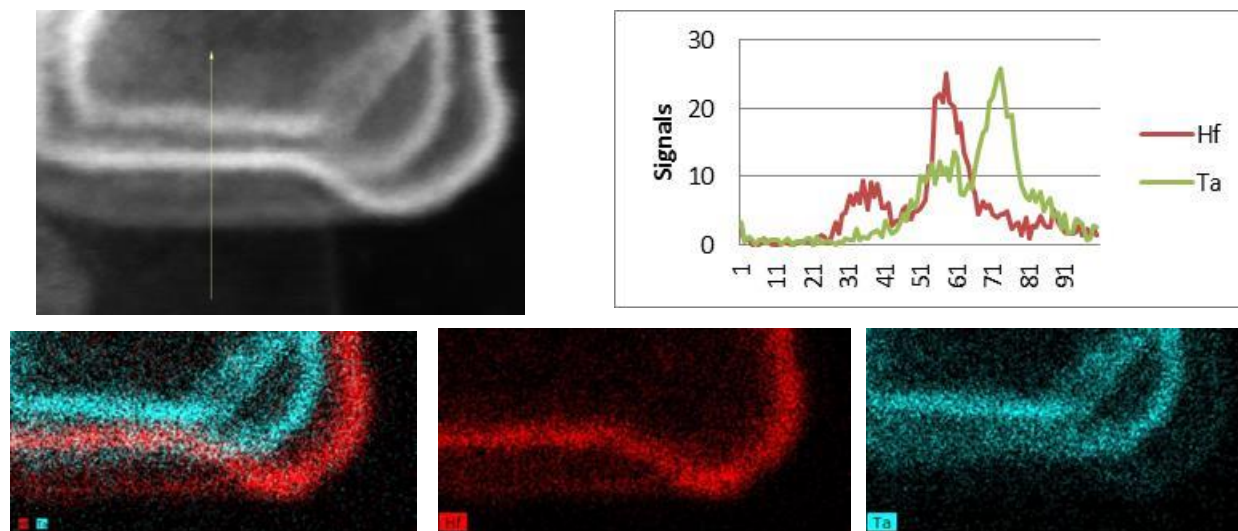
[3] W. Zhao, *Symp. Proc. the Material Research Society, 2002 Fall Meeting*, (2002), Vol. 738, pp. G7.15.1~6.



**Figures 1.** The extra PFETs in cross-sectional TEM were artifacts (indicating by Letter X) from a projection effect, in an adjacent row of SRAM PC gate, diminished with thinning of the TEM lamella.



**Figures-2** Demonstrated “project effect” of SiGe epi cluster diminishing, until critical dimensions can be confidently measured in a pull-up (PFET) in SRAM.



**Figures-3** XEDS elemental mapping and linescan revealed that the extra layers under PC gate stacks near an edge of STI, were Hf and Ta, not foreign materials; indicating a projection effect, due to undulation at the bottom of the long channel PC, in a thick TEM sample.