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Toward a fully integrated automotive radar system-on-chip in 22 nm FD-SOI CMOS

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Research Paper

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Abstract

Next-generation automotive radar sensors are increasingly becoming sensitive to cost and size, which will leverage monolithically integrated radar system-on-Chips (SoC). This article discusses the challenges and the opportunities of the integration of the millimeter-wave frontend along with the digital backend. A 76–81 GHz radar SoC is presented as an evaluation vehicle for an automotive, fully depleted silicon-over-insulator 22 nm CMOS technology. It features a digitally controlled oscillator, 2-millimeter-wave transmit channels and receive channels, an analog baseband with analog-to-digital conversion as well as a digital signal processing unit with on-chip memory. The radar SoC evaluation chip is packaged and flip-chip mounted to a high frequency printed circuit board for functional demonstration and performance evaluation.

Introduction

The automotive industry and its supply chain are currently undergoing a historic transformation. After decades of perfecting existing technology, the industry is currently working towards a fundamental transformation of individual mobility. In addition to new software-based business models, the trends towards connected vehicles and assisted and autonomous driving are considered to be the pillars of the automotive future [1]. Environmental sensing systems obviously play a central role and in addition to camera systems, sensors that provide more accurate speed estimates or simply work in poor lighting conditions, are increasingly being employed as the level of autonomy increases. Radar is such a technology that works reliably even in total darkness or against the sun.

Radar in itself is not a new technology but entered the automotive market some 20 years ago for comfort functions such as adaptive cruise control. Since then, sensor technology has developed considerably and today safety aspects are more important. Especially the safety classification of the New Car Assessment Program organizations requires for a good evaluation not only safety in crash tests but also systems that prevent accidents from happening in the first place. For example, assistants for detecting objects in the blind spot are standard equipment in new vehicles, as are lane change assistants.

Since 2020, emergency brake assistants are also mandatory, but not only for simple scenarios between vehicles but also for scenarios in which so-called vulnerable road users are involved, i.e. pedestrians or cyclists. From the point of view of radar sensor technology, this means ever higher demands on sensitivity and separation capability, which in direct comparison with adaptive cruise control (ACC) results in enormously dense point clouds. The detection, processing and classification, and finally the decision-making have to be done by the vehicle at very short notice. At the same time, to be able to equip also entry-level cars with radar sensors the costs need to be cut considerably. In order to achieve these cost targets, the industry is increasingly making use of economies of scale through platform concepts and, in particular, of cost reduction through integration.

This article discusses the challenges and opportunities of modern deep submicron complementary metal oxide semiconductor (CMOS) for single-chip radar (the section Deep submicron CMOS for single-chip radar) and presents test chip results collected on the way toward a fully integrated automotive 77 GHz radar transceiver chip (the section, Radar transceiver building blocks testchips). The first paper [2] covers the technical implementation details and measurement results of this radar chip realized in a 22 nm CMOS technology, while this article expands on the digital interference measurement results (the section, Automotive radar SoC evaluation chip) and shows first radar measurements of the chip mounted on a dedicated functional demonstrator board (the section, Automotive radar SoC evaluation chip application).

Deep submicron CMOS for single-chip radar

These two paradigms, platform concepts and integration, have proven to be successful when looking at the evolution of automotive radar sensors.

Fig. 1. Bosch radar sensor evolution, from adaptive cruise control (ACC) to long- and mid-range sensors (LRR/MRR) as well the latest generation 5.

Automotive radar sensor evolution

A sensor that is simple in its function as a distance cruise control from today's point of view can be seen on the far left in Fig. 1. Back in the early 2000s, it was largely constructed discretely from individual high-frequency components. About a decade later, the so-called long-range sensor 3 was introduced for ranges up to 250 m. Here the whole high frequency part was already integrated into a silicon germanium (SiGe) transceiver chip, including the voltage-controlled oscillator (VCO) that generates the transmit signal (Fig. 2(a)). The VCO was externally controlled by a phase locked loop (PLL), which was referenced to a 19 GHz dielectric resonance oscillator. The PLL along with the baseband processing was performed in a Bosch radar application specific integrated circuit (ASIC) on a complementary low-frequency board, while the radio frequency (RF) chip was mounted and wire-bonded to the RF circuit board using chirp-on-board technology. About 5 years later, the mid-range sensor with dedicated transmit and receive chips followed, both implemented in SiGe, but here the transmit chip also contained the VCO and provided the local oscillator signal to the receiver chip (Fig. 2(b)). The intermediate frequency (IF) receive signals were connected to a next-generation Bosch radar ASIC for filtering and analog to digital conversion (ADC), before being digitally processed in a third-party microcontroller chip. From the dielectric lens-based concept, the development went towards a planar antenna system, which allows a hidden installation behind bumpers. Its range was specified up to 160 m in front mode but could also be used for rear/side applications with a different antenna layout.

In Bosch's current fifth-generation a SiGe bipolar-CMOS (BiCMOS) single monolithic microwave integrated circuit (MMIC) with three transmitters and four receivers is used, which includes a ramp generator, the IF processing and the ADC, while the digital signal processing takes place in a third-party microcontroller (Fig. 2(c)). For the first time, chirp sequence modulation is applied, which detects position, speed and direction of motion in a single radar measurement. It supports adaptive cruise control as well as automatic emergency breaking and sub-functions of automated driving.

While automated driving is reported [3] to require an average of three radar sensors per vehicle at total costs of $210 for Level 0 to Level 2 (2015), it is estimated that more than twice as many sensors will be required for Level 5 (2025), at roughly the same total cost. The costs per near range sensor will therefore need to be halved from $60 in 2015 to less than $30 in 2025. Moreover, in order to be eligible for safety-critical applications, the functional safety concept requires monitoring of many parameters and live evaluation during the sensor operation. In an integrated solution, this can be achieved with less effort and more extensively than in a multi-chip solution. Therefore, a system-on-chip (SoC), which combines both the analog front-end and the digital signal processing, is the logical step for the next radar generation.

Challenges in the digital integration of SoC development

Today's CMOS technologies are increasingly being considered to continue this trend towards further monolithic integration. While 55 nm CMOS and BiCMOS nodes are reported to feature 700–1000 k gates/mm^2 [4], 28 nm CMOS achieves 4200 k/mm^2 [5], 22 nm achieves 5500 k/mm^2 and 14 nm even 9000 k/mm^2 [6]. While the highest digital integration would require the smallest nodes, the analog and the high-frequency performance tends to degrade with smaller nodes. Conventional bulk CMOS, which is a common technology for semiconductor nodes down to 28 nm, has the simplest layer structure and employs the conventional approach of scaling the gate oxide thickness and the channel length simultaneously without requiring double patterning. However, because it tends to have static leakage currents, more complex digital designs require more complex layer structures. The so-called FinFET technology, for example, encloses the channel with three-dimensional gates and thus provides better off-isolation, and the so-called fully-depleted silicon over insulator (FDSOI) technology isolates the entire transistor from the substrate via an oxide layer (buried oxide) and thus also reduces parasitic drain currents.

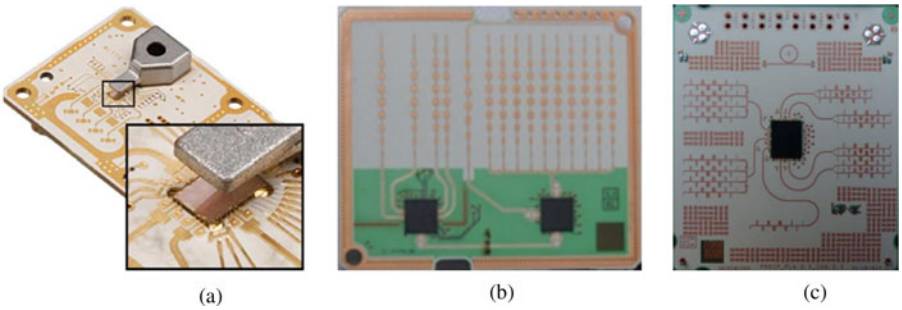

Fig. 2. Bosch radar high-frequency boards with transceiver semiconductor chips.

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Table 1. Cost comparison of deep submicron CMOS technologies

Technology	28 HKMG	22 FD-SOI	14 FinFET
kGates/mm^2	4200 [5]	5500 [6]	9000 [6]
Est. Cost/100 MGates [7]	$.90	$1.06	$1.43
# Mask layers [6]	n/a	40	60
Transit frequency f_T/f_{max} [8]	315/360 GHz	350/325 GHz	250/300 GHz

This technological effort obviously comes at a cost; a 22 nm FD-SOI wafer for example needs about 40 lithography masks, while a 14 nm wafer with FinFET technology needs about 20 masks more [6]. The higher digital gate density notwithstanding this actually makes digital gates more expensive in smaller technology nodes and are reported [7] to increase from $.90 for 100 million gates on a 28 nm chip to, $1.06 in 22 nm and $1.43 in 16 nm. While 28 nm bulk CMOS, therefore, may be the most cost-effective for many designs, a thorough tradeoff between analog and digital performance and cost has therefore to be made, the key parameters for this tradeoff are summarized in Table 1.

Furthermore, these more advanced technologies have increasing demands on the layout in terms of manufacturability (design for manufacturability, DFM), which is reflected in the number of design rules. A statistic [9] shows an average of about 1000 rules for a 65 nm process and nearly 10 000 for a 14 nm process. These design rules are no longer black and white below 28 nm bulk CMOS but generate a yield score which has to be optimized. It is getting more and more difficult even for experienced circuit designers and layout engineers to master all design rules, and since many of the rules are interdependent, much more trial & error iterations are needed in the design phase. Since these design rules also differ from technology to technology, a second source or a technology transfer comes with great effort.

The great effort for DFM is also reflected on the intellectual property (IP) side. While standard blocks such as pads, I/O libraries or memory generators are typically provided by the foundries, the increasing complexity of a SoC requires the use of third-party IP for certain functions, such as clocking, digital interfaces or computing cores. The automotive sector has significantly more stringent liability requirements, has to work within wider temperature ranges for components employed close to the engine or exhaust, and requires the IP provider to guarantee long maintenance times, e.g. for process design kit updates. Because the automotive sector is a comparatively small market compared to the consumer sector, the required IP is not always found in the target technology.

Apart from handling, integrating and verifying the multitudes of IP macros needed for an SoC – other examples are safety and security modules, general purpose data converters, debugging interfaces, and so on – the SoC design is also a challenge from the perspective of requirement engineering. In contrast to a multi-chip solution, where the signal processing takes place in a dedicated processor chip, for example, the computing power and the available memory have to be agreed on with the customer early on in the development stage. Any misalignments in the early definition of the resources are a serious risk since subsequent changes are associated with high costs and long cycle times further down the road.

Finally, the combination of highly sensitive analog circuitry and fast switching digital circuitry on a single chip requires elaborate integration concepts. On the one hand, the circuits are prone to interaction, e.g. electrical interference via the power supply or the semiconductor substrate. On the other hand, the heat that could conventionally be distributed over several chips was therefore dissipated well and is now concentrated in a single package and needs to be coupled to the heat sink of the sensor via a much smaller area. This places special demands on the thermal management, and in particular, on the package and on the printed circuit board (PCB) design, which, by the way, also needs to ensure the routeability of the multiple interfaces of the SoC.

In summary, automotive radar SoCs of the next generation will be increasingly complex and expensive to develop. Generally, to leverage the capabilities of deep submicron technology nodes, the product development of an SoC with all its domains like architecture, specification, software development, prototypes, validation, IP purchasing etc. is expected to become increasingly expensive, e.g. $40 M for a typical 40 nm design, $70 M for 22 nm, and $100 M for 14 nm [7]. Compared to the development of frontend chips with dedicated microprocessors for the first automotive radar generations, the commitment to enter the SoC era with deep submicron CMOS for the next radar generation has become substantially higher.

Millimeter wave performance of deep submicron CMOS

In addition to the aforementioned development challenges, the most prominent reason why radar SoCs have not yet penetrated the automotive market is the transistor speed of the underlying CMOS technologies. As a rule of thumb, their transit frequency should be at least three to five times the carrier frequency of the circuit, which corresponds to 240–400 GHz for the 78 GHz automotive radar band. While 90 nm CMOS reached transit frequencies about 150 GHz, also 65 nm achieved only 200 GHz and it was not until the 40 nm node that the first CMOS technologies entered this area. Today, the transit frequency of state-of-the-art CMOS semiconductor nodes such as 22 nm FDSOI is on par with fastest SiGe bipolar processes from a few years ago, reaching transit frequencies up to 350 GHz.

Even though the transit frequency of technology can give a first indication of the achievable speed of analog circuits, there are a number of other technological features that have so far made CMOS unattractive for radar. For example, transistors could not be stacked for high output voltages and thus high output power, the top metal layers were not suited for high-quality passive components (transmission lines, inductors) and the high flicker noise corner frequency made low noise design difficult. As can be seen in Table 2, this has apparently changed with 40 nm and 28 nm nodes as more and more publications report decent performance of central radar building blocks. Two of the most important performance parameters for radar are the transmit power and the receiver noise, which together define the link budget of the system and thereby directly influence the achievable range of the sensor.

With regard to the transmit power, designs in current CMOS technologies achieve 12dBm and more at high ambient temperature (125C), which is a typical value also reported for SiGe-based designs. As for the receiver noise, the comparison of the state of the art yields a more differentiated image, mainly because of two reasons. First, there is a fundamental tradeoff in the receiver

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Table 2. Radar transceiver key metrics at 125°C junction temperature

	Transmitter				Receiver		
	Technology	Transmit powerdBm	Efficiency		Technology	Noise figuredB	P1 dBdBm
CMOS	22 nm [10]	12	15% PAE	CMOS	22 nm [10]	10	
	28 nm [11]	12	88 mW, 13% PAE		40 nm [12]	11	
	28 nm [13]	18	609 mW		45 nm [14]	18	−7
	40 nm [15]	13.8					
	45 nm [14]	10.8					
SiGe	Bipolar [16]	11.7*		SiGe	Bipolar [17]	12*	−1.2
	BiC130 [18]	14.3			BiC130 [19]	9.5* (10 M)	−5
	BiC130 [19]	13*			BiC180 [20]	15 (1 M)	−5
	BiC180 [20]	11.5					

Values denoted with * are given at ambient temperature
Noise figure reported at 1 MHz.

design between noise and linearity, and it is construed differently depending on the overall transceiver system design. Second, the 1 MHz frequency point at which the spot noise figure is reported is in the area of the kink between flicker noise and white noise for many CMOS technologies and which makes the 1 MHz spot inherently sensitive to the technology. This higher noise figure can be mitigated because of advances in the analog baseband and analog-to-digital converters combined with higher chirp slopes. This shifts distant targets with low backscatter to higher frequencies, where the noise figure is typically lower. Also, a higher digital density with more radar memory enables higher integration times which also lowers the effective noise floor. From the high-frequency point of view, it follows that today's CMOS technologies are technically viable solutions for automotive radar.

Radar SOC evaluation in 22NM FDSOI technology

Given the aforementioned SoC development effort, a series of simpler test chips are typically needed to pave the way toward an SoC design that meets the performance expectations for next-generation radar sensors. As discussed in the previous chapter, the high-frequency transmit and receive performance is a key concern in the smallest technology nodes, which strongly suggests upfront validation.

Radar transceiver building blocks testchips

With smaller CMOS technology nodes, the transistor breakdown voltages tend to decrease, which is a major disadvantage for the design of amplifiers with high output power. Therefore, two power amplifiers with different topologies were evaluated as test chips, a stacked power amplifier and a capacitively neutralized power amplifier. The stacked amplifier employs multiple transistors whose drain-source voltages are in series to increase the output voltage swing. The operating point at the gates is adjusted by means of a resistive divider and the impedances at the gate terminals of the stacked transistors are adjusted in such a way, e.g. by additional capacitances, that the drain-source voltages of all stacked transistors add up in phase. On the other hand, the functional principle of the neutralized amplifier is solely based on capacitive feedback within a single common source amplifier stage. Multiple stages are typically cascaded to maximize the small-signal gain in the first stages and saturate the final stages, for example through inductive coupling with scaling of the transistor size from one to the other stage. In direct comparison of the two topologies in a partially depleted 45 nm CMOS technology [21], both amplifiers achieved a high peak output power of 15dBm. However, the neutralized amplifier is less complex and thus tends to be a more robust design over process, supply voltage and temperature variation (PVT), which is crucial for automotive semiconductor designs. This was confirmed with the stacked amplifier being severely decentered (67 GHz), while the neutralized amplifier was much closer to the 76–81 GHz target band (73 GHz). The simpler neutralized amplifier eventually achieved satisfying output power above 10dBm, under high-temperature conditions and after subtraction of estimated package losses.

Based on these considerations, this neutralized amplifier topology was used for a two-stage transmitter testchip (Fig. 3) in a fully depleted 22 nm CMOS technology. At 76 GHz a saturated output power of 10.2 dBm is achieved (105°C, at pad), which drops to 9.4 dBm at 81 GHz. While there is still room for high-temperature improvement, 11 dBm were achieved across the 76–81 GHz band at ambient temperature, which allows for reasonable radar operation in a SoC.

In the same run also a receiver was taped out (Fig. 4), which converts the single-ended echo signal to differential over an on-chip Marchand balun, amplifies it with a highly linear common gate low noise amplifier and mixes it into the baseband with the help of a passive, double-balanced, homodyne mixer. The current signal is subsequently translated to the voltage domain by a transimpedance amplifier. The whole chain has a receive gain of about 15 dB, as shown here with only a few decimals dB temperature dependency. The high linearity can be recognized by the fact that the gain curve over the input power is flat up to −3 dBm. This is important in radar systems for two reasons: on the one hand to minimize the influence of the crosstalk from the transmitter to the receiver, which can reduce the sensitivity for weak or distant objects. On the other hand, to minimize intermodulation products that could be identified as ghost targets by signal processing and leading to emergency braking. Despite the high linearity in the form of the 1 dB compression

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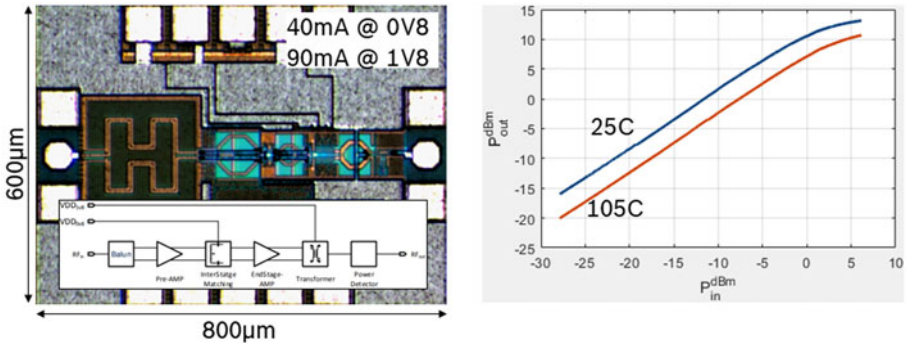

Fig. 3. Two-stage neutralized power amplified in 22 nm FD-SOI CMOS. Left: chip micrograph. Right: output power at 76 GHz (probes and input balun deembedded).

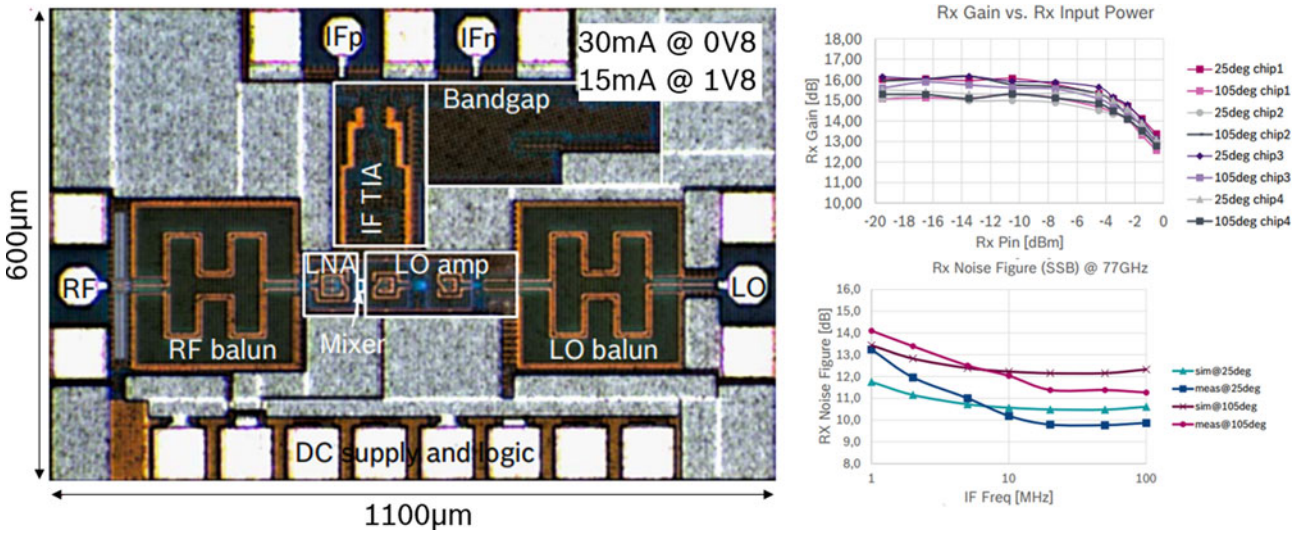

Fig. 4. 77 GHz receiver frontend in 22 nm FD-SOI CMOS.

point of about −3 dBm, a competitive figure of around 12 dB was achieved. Together in this combination, this results in a dynamic range which is several decibels above the state of the art and thus promises a good radar system sensitivity.

Automotive radar SoC evaluation chip

The next step after the performance evaluation of individual modules is the validation of their integration at the top level. This is perhaps what most reservations and concerns arise from in the context of monolithic integration of a radar transceiver along with its digital backend: not only the coupling between analog circuits needs to be minimized but also needs the sensitive analog frontend to be isolated from the fast-switching digital logic. This analysis is the purpose of the radar SoC evaluation chip presented in this section and depicted in Fig. 5. In addition to the aforementioned transmit and receive macros, which were each inserted twice for a two-by-two virtual channel configuration, all building blocks for radar operation are present. The frequency synthesis is performed on-chip using a digitally controlled oscillator at 26 GHz, which is upconverted to the 78 GHz band using an on-chip frequency tripler. The receiver also contains an analog baseband with configurable high pass and anti-aliasing filtering as well as an analog-to-digital converter. The digitized receive data can subsequently be processed in an on-chip digital signal processing chain with fast Fourier transform (FFT), noncoherent integration and constant false alarm rate (CFAR) detection threshold adaptation. The packaged chip measures 7×7 mm^2, with silicon area of 14 mm^2 and the analog frontend dissipates about ca. 0.7 W at 100% duty cycle (all four channels, including the DCO and the frequency tripler). The millimeter-wave chip performance is evaluated using a measurement assembly on a dedicated characterization PCB with WR12 waveguide connectors. A thermal head can be attached to the surface of the chip package, which allows for controlling the operating temperature within a wide range. Further details regarding both the implementation and the achieved analog performance of the demonstrator chip can be found in [2], a summary is given in Table 3.

As stated before, the major concerns that should be addressed with this radar SoC evaluation chip were the crosstalk between the switching digital circuitry and the sensitive analog frontend. For the evaluation of such digital interference, a randomized FFT and CFAR test mode is implemented into the chip. A worst-case stimulus of FFT, CFAR, and RAM operating at full load can be activated with on/off periods at configurable multiples of the digital clock of 1/400 MHz. In order to isolate spurs from a digital activity from other spurs in the system, the differential baseband signal is evaluated directly in the analog domain with a spectrum analyzer. The spectrum analyzer resolution bandwidth is set

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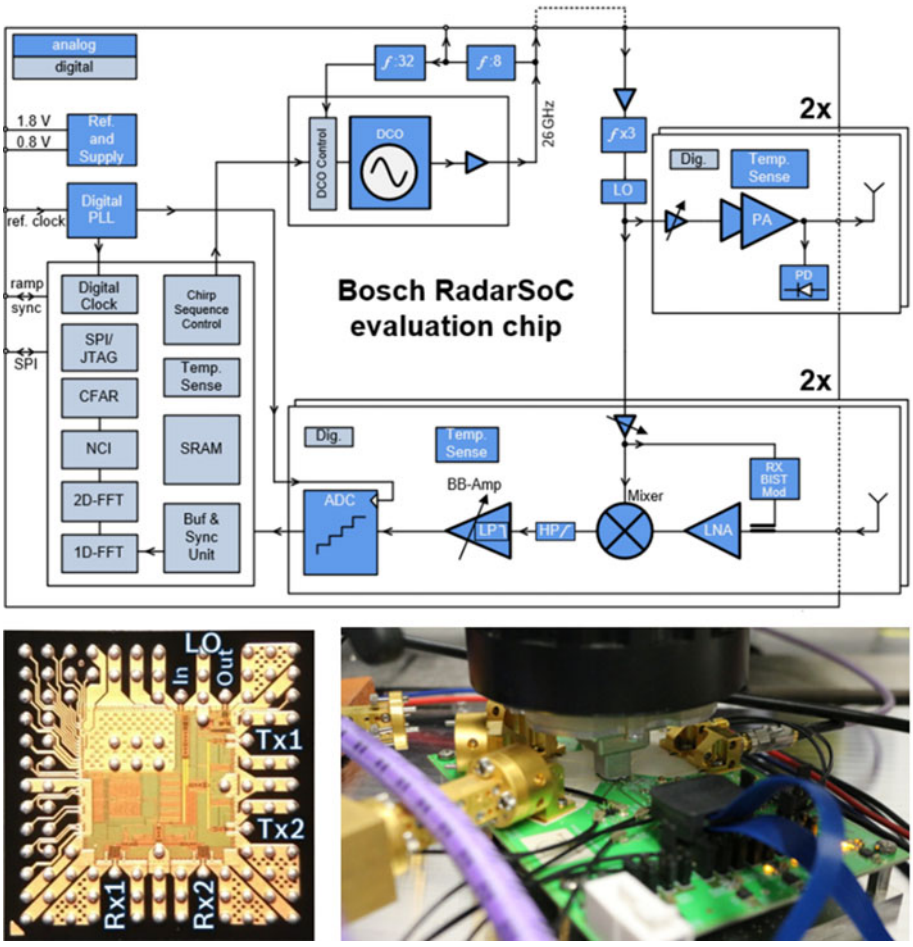

Fig. 5. Radar SoC evaluation chip in 22 nm FD-SOI. Top: block diagram. Bottom left: die photo. Bottom right: lab characterization assembly.

narrower than a typical radar modulation bin width, which makes spurs visible that are below the typical noise floor and the detection threshold.

Figure 6(a) shows the receiver idle measurement as a reference for the following considerations. The spurs up to around 2.5 MHz are attributed to an auxiliary power-over-ethernet adapter, that powers the measurement control board via a 48–12 V switched mode power supply. The dent around 4 MHz and the noise increase towards smaller frequencies is an artifact of the spectrum analyzer's intermediate frequency path, while the decrease towards higher frequencies is due to the 20 MHz anti-aliasing filter in the receiver baseband (−18 dB per octave). The RAM pseudo activity, when activated, always has a duty cycle of 50%, and in Fig. 6(b), a configuration with 15 out of 30 active cycles is shown. This modulates the power supply at a frequency of 400 MHz/30 = 13.3 MHz, which causes the spur in the received spectrum.

Table 3. Radar SoC evaluation chip performance summary (from [2]).

Parameter	Condition	Value	Unit
Transmit power	RF = 76–81 GHz, T = 25C	11.5±0.5	dBm
incl. package loss	RF = 76–81 GHz, T = 125C	7[1]	dBm
Channel isolation	Tx_2–Rx_2 (worst case)	17–20	dB
	Tx_1–Rx_1 (best case)	35–45	dB
Rx Frontend gain	RF = 76–81 GHz, T = 25C	13–14	dB
1 dB compression	T = 25C	−3.5	dBm
Noise Figure	IF = 10 MHz, T = 25C	12.8	dB
incl. package loss	IF = 10 MHz, T = 125C	14.5	dB
DCO phase Noise	IF = 1 MHz (26 GHz)	−100	dBc/Hz
	IF = 10 MHz (26 GHz)	−125	dBc/Hz

[1]limited by LO drive, power amplifier expected to deliver 9dBm at appropriate input power.

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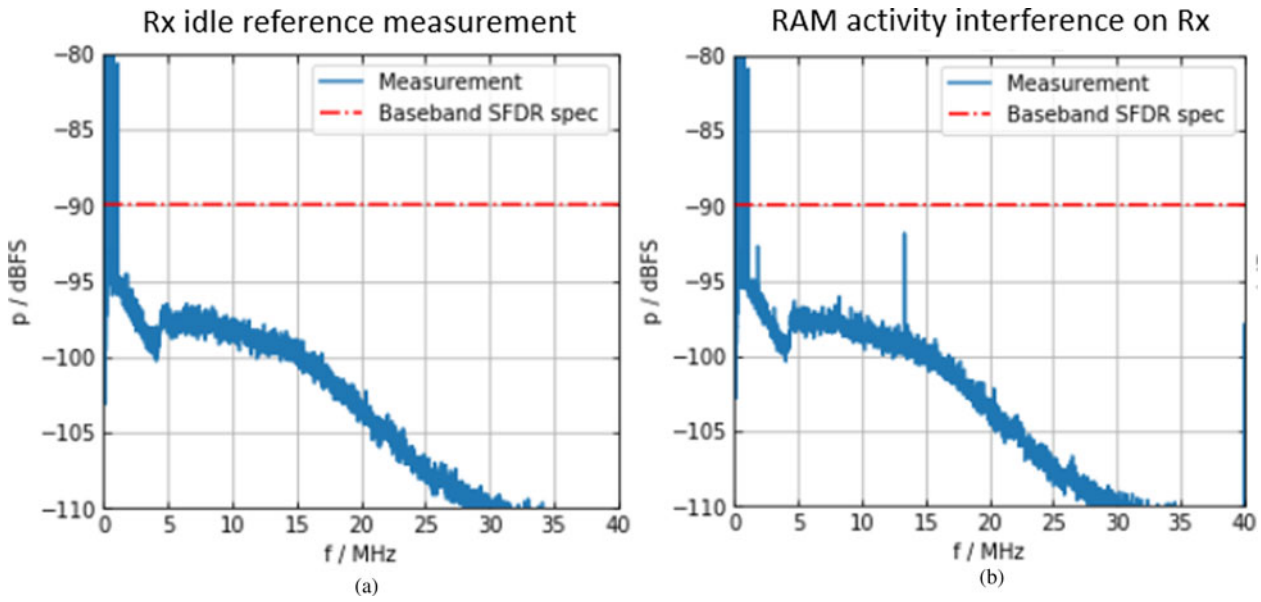

Fig. 6. Digital interference measurement. (a) Reference measurement without digital activity. (b) *Rx* measurement with pseudo-random activity in the on-chip memory.

The FFT and CFAR interference test modes are also controlled with a counter and are active as long as the counter value is lower than a programmable 8-bit threshold and inactive during the remaining period of a total of 255 clock cycles. Figure 7 shows the baseband spectra with two counter settings. In (a) it is set to the maximum value of 255, i.e. both FFT and CFAR are permanently active (100% duty cycle), in (b) it is set to 128, i.e. both FFT and CFAR are partially active (50% duty cycle).

- The permanently active case with constant power dissipation shows no spurs, while the partially active case exhibits 400 MHz/256 = 1.6 MHz spaced spurs, particularly in the upper half of the baseband spectrum. Consequently, a significant

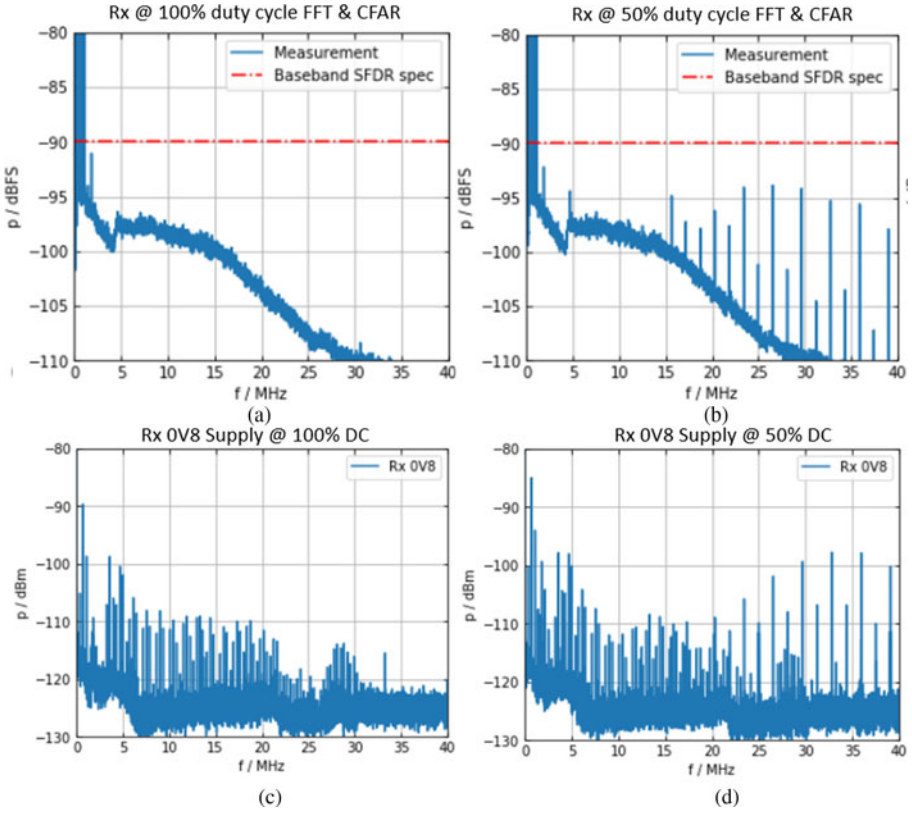

Fig. 7. Digital interference measurement with FFT& CFAR operation. (a) and (b) *Rx* output spectrum with 100% and 50% duty cycled activity. (c) and (d) corresponding 0.8 V *Rx* supply voltage measurement.

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part of the observed interference is because of the modulation of the digital power dissipation and not because of the digital activity itself.
- When the anti-aliasing filter is reduced from 20 MHz to 5 MHz, the receiver noise floor lowers accordingly and more spurs become visible in this frequency band. The higher frequency spurs are not affected by the anti-aliasing filter cutoff frequency; however, most spurs are observed to scale with the baseband amplifier gain. A coupling of the modulated digital power dissipation into the baseband amplifier, rather than into the millimeter wave frontend, is therefore likely.
- The power supply in the permanently active case (Fig. 7(c)) shows spurs below 15 MHz in the same order of magnitude as in the partially active case (Fig. 7(d)), while spurs are only visible in the baseband in the partially active case. Furthermore, the amplitude-frequency responses differ between the 1.6 MHz spaced spurs on the power supply and in the baseband. A coupling path different independent of the receiver power supply, therefore, seems to exist.

Since the baseband amplifier is placed in the floorplan right on the boundary to the digital part, a direct coupling path from the digital to the baseband, e.g. via the substrate, is easily conceivable. However, since any observed spurs are below the typical radar receiver idle channel spur specification limit of −90dBFS (e.g. [22]) the isolation concepts employed between the analog and digital domains have proven to be sufficiently effective.

Automotive radar SoC evaluation chip application

Based off of the promising results of the radar SoC evaluation chip, a first functional demonstrator was built (Fig. 8(a)). The radar SoC evaluation chip is soldered to a high-frequency substrate with a two-by-two channel patch antenna array. This board also features a switched mode power supply, as well as an external PLL that can serve as a clean reference without any chip-internal digital interference. The functional demonstrator board is attached to the same backend board as used for the characterization, which features a processing unit running Linux, e.g. for remote control and data capture via Ethernet.

Since the closed-loop on-chip DCO control loop is not yet functional, the actual frequencies of the DCO were measured for each of the 16-bit DCO control words prior to the functional operation of the demonstrator. Any desired chirp configuration can subsequently be generated by offline synthesizing and storing the respective DCO control words in an on-chip memory, which the on-chip sequencer loops across in radar operation. Figure 8 shows an example measurement of such a 16 MHz/µs chirp with 160 MHz bandwidth using a spectrum analyzer.

With this ramp configuration, a radar measurement is performed in the lab as shown in Fig. 8(c); the antenna boresight

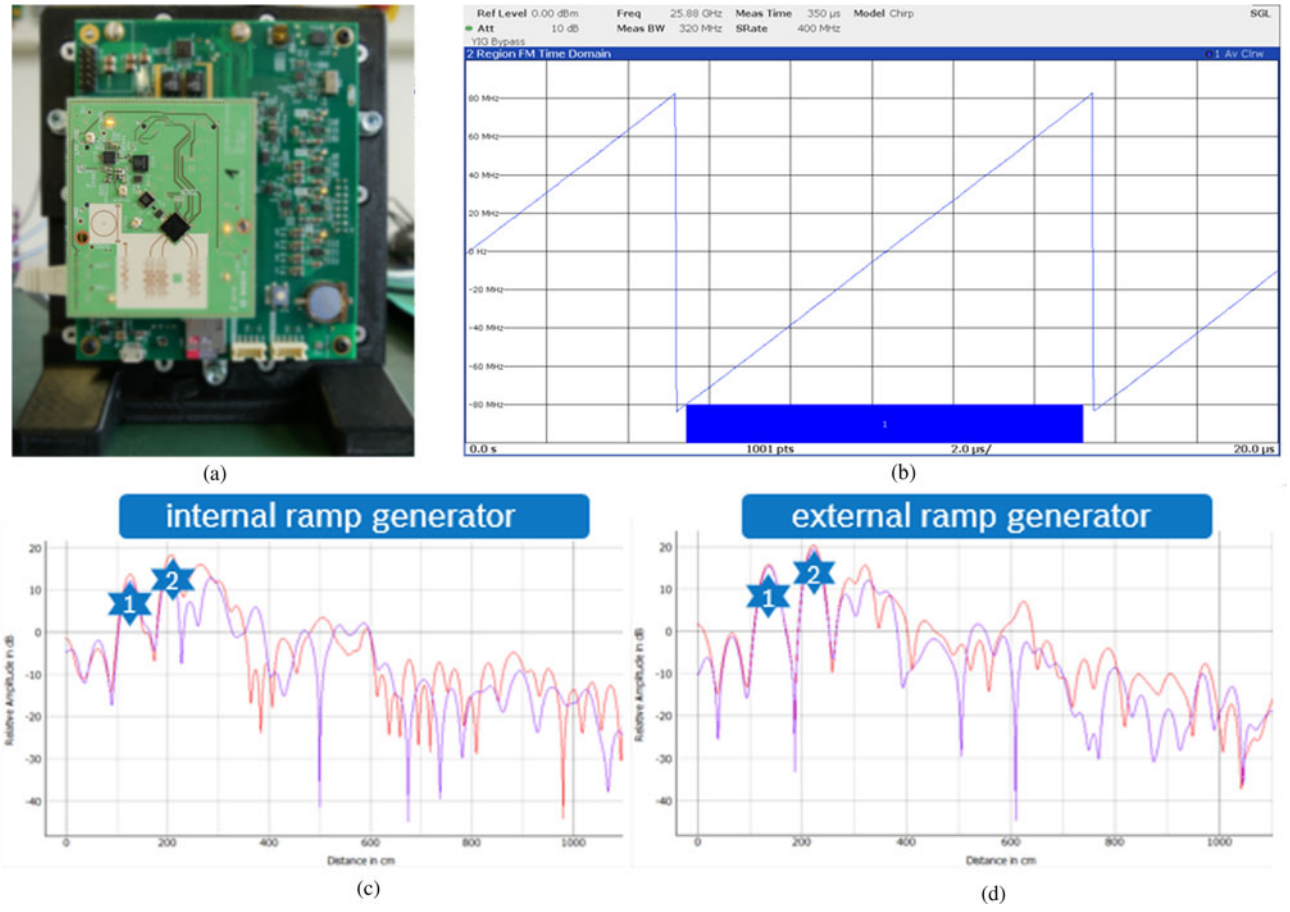

Fig. 8. Radar SoC functional demonstrator. (a) Demonstrator PCB with backend board. (b) Measurement of synthesized DCO ramp. (c) Radar measurement with DCO ramp. (d) Radar measurement with ramp generated with external PLL.

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direction is towards the ceiling. The echo in the range spectrum marked as star 1 is due to a solder smoke absorber that is mounted on the bench in about 120 cm distance, the reflection at star 2 is the ceiling, echos beyond that distance are multi reflections in the room. The same echoes are visible with similarly good separability in the measurement repeated with the on-board reference ramp generator. However, the final evaluation of the radar SoC performance can only be done inside an anechoic chamber with a radar target simulator.

Conclusion

Over the past two decades, the automotive radar sensor has evolved from serving comfort features in high-class vehicles, to being a crucial safety component mandatory even in entry-level cars. To increase the affordability of the technology, more and more functionality has been combined in fewer semiconductor chips, such that today the market is facing the monolithic integration of the high-frequency frontend and the digital signal processing. While the development complexity for such a radar SoC is enormous, e.g. in terms of development cost, requirements engineering or IP management, the high gate density of today's advanced semiconductor nodes helps leverage cost benefits. This article and the presented radar SoC demonstrator chip showed that from a high-frequency perspective, deep submicron CMOS is suited for the 76 GHz automotive radar band. It was also shown that general reservations of the limited isolation between the fast-switching digital logic and the sensitive analog circuitry are justified, yet any observed interference was several decibels below the specification limits. A functional demonstrator featuring the radar SoC evaluation chip was presented for the assessment of the real-world performance, of which first lab measurements demonstrated its functionality. Within the next couple of years, a prevalence of single radar chip-based sensors can therefore be anticipated.

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