

In-Situ Investigations of Individual Nanowires within a FIB/SEM System

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The move from planar CMOS-based microelectronics and advanced device structures like FinFETs and FD SOI structures to devices with 1-dimensional nanostructures (Si, Ge, III-V semiconductors) requires fundamental studies of nanostructures and innovative approaches to integrate the new materials and structures into microelectronic products. The approach of nanowire-devices for reconfigurable field effect transistors (RFETs) includes Schottky junctions that have to be designed and characterized.[1]. Due to their extraordinary physical properties, silicon nanowires have a great potential in application as nanoscale transistors and sensors. These future technologies and products provide new challenges to analytical techniques with high spatial resolution, particularly TEM and the respective sample preparation with minimal sample damage [2]. In this paper, we are presenting a nanoanalytical study of silicon nanowires which are completely surrounded by a gate oxide as well as Schottky barriers.

The Si and Ge nanowires were synthesized using the vapour-liquid-solid (VLS) growth on Si or on Ge/Si substrates. A thin Au film was deposited onto these substrates, and annealed to create Au nanoparticles which act as catalyst for the nanowire growth. The nanowires grow as “forests” with distributions for growth orientation and diameter.

In a second processing step, the nanowires were removed by solvent assisted ultrasonic vibration, and subsequently spray-coated onto Si/SiO₂ wafers followed by an anneal step that produces a thin oxide layer around the nanowires. Using an e-beam lithography/etch patterning process, sections of the oxide shell were selectively etched and Ni-electrodes were deposited. A subsequent anneal step was performed to silicidize the nickel. The nickel silicide forms a sharp junction in the nanowire. These Schottky junctions are the basis for reconfigurable FETs [1,3].

We characterized the morphology of the nanowires using a FEI Helios FIB/SEM system. Electrical characteristics are obtained *ex situ* on the Schottky-barrier devices.

Furthermore, we used the FIB/SEM technology to prepare and to characterize specific individual Si or Ge nanowires *in situ* based on properties like their crystallographic orientation, their length or their diameter. In contrast to the fabricated junctions, the nanowires in the “forests” were in the as-grown state. Applying a micromanipulator (FEI EasyLift), the nanowires were extracted from the growth surface and put onto test structures inside the FIB/SEM tool.

The results obtained by *in situ* measurements were compared to those obtained with nanowires on Si/SiO₂ contacted with nickel.

The study of individual, pre-selected nanowires and a comparison with the respective properties in manufactured device structures allows improving yield and quality of high performance devices for future electronics [4].

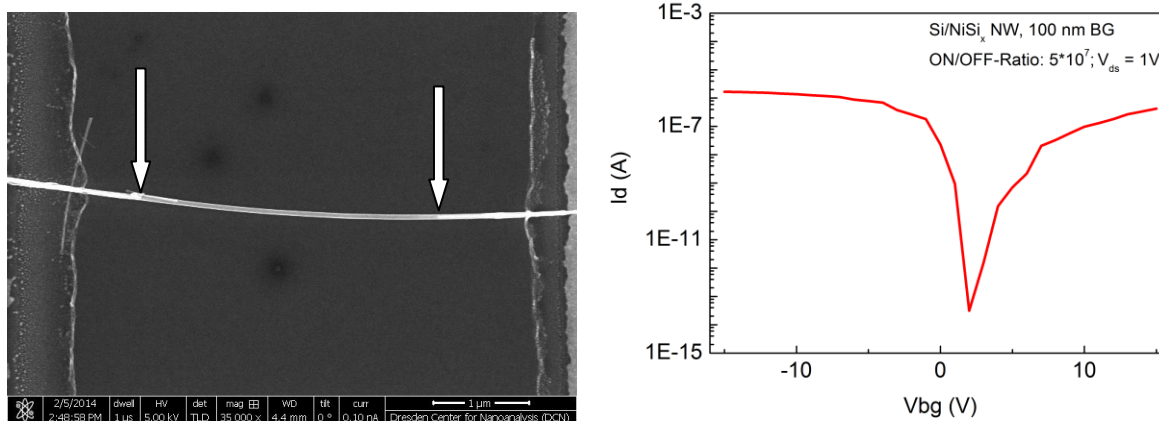


Figure 1. Left: SEM image of a Si-NW with two Schottky junctions (arrows). Right: Ex situ measured current-backgate voltage characteristics of prepared $NiSi_x$ -Si-NW with oxide shell.

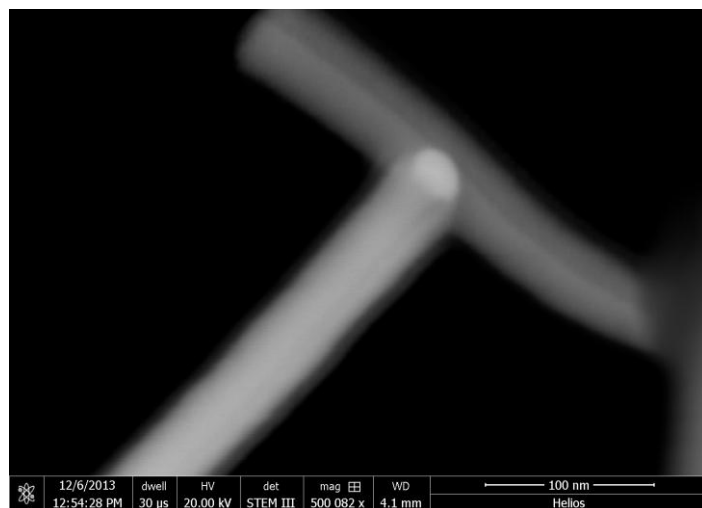


Figure 2. Pulled-out Si-NW attached to manipulator. The bright particle is the Au catalyst.

[1] A. Heinzig *et al.*, Nano Lett. **13** (2013), p. 4176.

[2] S. Banerjee *et al.*, Electron Microscopy Conference, Krakow, Sept 2014.

[3] A. Heinzig *et al.*, Nano Lett, **12** (2012), p. 119.

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