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Microscopy of Materials Used In the Semiconductor Industry

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Recent advances in analytical electron microscopy and specimen preparation techniques [1-3] have made the investigation of materials used in semiconductors significantly easier than those available to the industry over a decade ago. Routine evaluations of semiconductor devices are now possible even in a manufacturing facility. Developments in focused ion beam milling techniques [4], ultra high-resolution microscopy and micro-chemical analyses [5-6], are affording a better understanding of the microstructure of materials, used in microelectronic devices, and its relationship to their properties and behavior at the nanometer node. This paper provides illustrations of using electron microscopy to address materials issues in semiconductors.

Example 1: The gate dielectric process is arguably the most critical challenge facing the physical scaling and extendibility of SiO_2 as the gate dielectric of sub-micron MOSFETs. It is shown that a high quality gate oxide, called G^3 oxide, can be made with a pristine Si/SiO_2 interface that is free from localized strain gradients as shown in Figure 1.

Example 2: Figure 2 shows a multilevel structure with copper metallization and intermediate layers of dielectric from a device used in cellular phones. The copper/dielectric interface quality and the metallization microstructure are important for assessing device reliability.

Example 3: Vias connect various metal layers in a semiconductor device. In this example (Figure 3), TEM was used to isolate a singular via that showed high contact resistance; an analysis of the W-plug via/Al-conductor interface showed a void. In another study, EDS analysis showed an anomalous layer on top of the W-plug via.

Example 4: Figure 4 shows an Al_2O_3 film that has been grown on GaAs for use as a gate dielectric, as part of an effort focused toward the development of next generation high-power, high-frequency RF devices for use in applications such as cable television base stations. Using TEM imaging, EDS, and CBED with this FIB prepared sample, it was determined that the crystalline lattice of the GaAs substrate directly below the oxide film has been disrupted and appears to have an amorphous structure that extends for several nanometers below the oxide film.

References

[1] B. Fultz and J. Howe, TEM and Diffractometry of Materials, Springer, 2002
[2] D. Williams et al., X-Ray Spectrometry in Electron Beam Instruments, MAS, 1993
[3] A. Rosenauer, TEM of Semiconductor Nanostructures, Springer-Verlag, 2003
[4] L. Giannuzzi and F. Stevie, (eds.), Introduction to Focused Ion Beams: Instrumentation, Theory, Techniques and Practice, Springer, 2004
[5] D. Joy et al., Principles of Advanced Electron Microscopy, Plenum, 1986
[6] K.N. Hooghan et al, The Electrochemical Society, Inc., Pennington, New Jersey, PV 2002-3, p. 276 (2002).

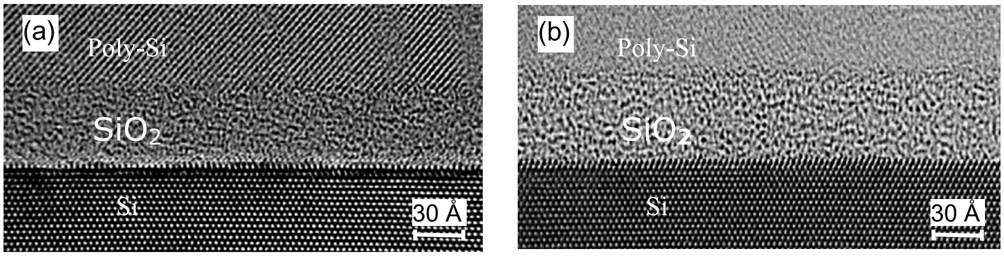

Fig. 1. HRTEM image of the Si/SiO_2 interface for (a) conventional and (b) G^3 gate oxides. Absence of dark bands for the G^3 oxide indicates formation of a strain free Si/SiO_2 interface. (Courtesy P.K. Roy)

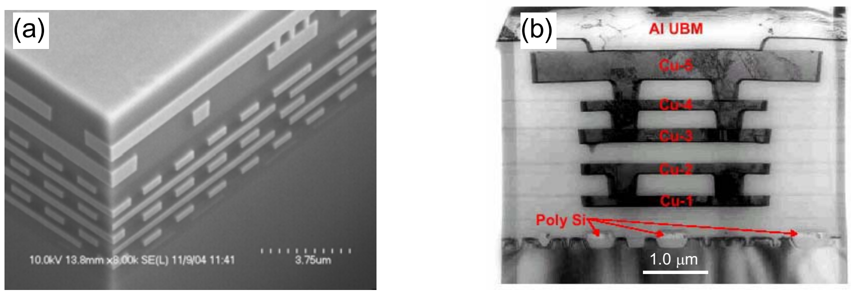

Fig. 2. Images of a multilevel copper interconnect structure from a semiconductor device used in mobile cellular phones. The samples were prepared by FIB and imaged using (a) SEM and (b) TEM (Courtesy V. Ryan).

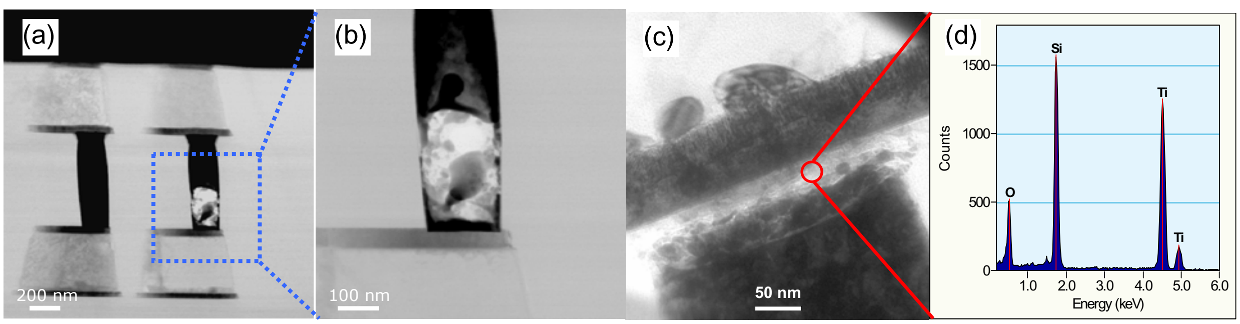

Fig. 3. (a) and (b) STEM images of a tungsten via that showed high resistance due to the presence of a void. In another study, (c) EFTEM imaging and (d) subsequent STEM/EDS analysis showed an anomalous layer on top of a tungsten via that also produced a high resistance condition.

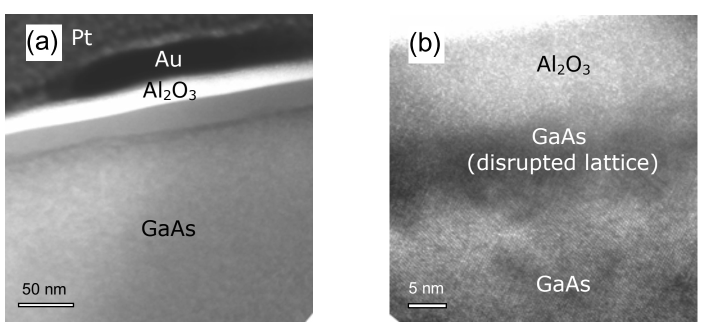

Fig. 4. EFTEM images of an Al_2O_3 film that has been grown on GaAs for use as a gate dielectric showing that the crystalline lattice of the GaAs substrate directly below the oxide film has been disrupted and appears to have an amorphous structure that extends for several nanometers below the oxide film. (Courtesy F. Yang)

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