Structural and Compositional Properties of Recrystallized CdS/CdTe Thin-Films Grown on Oxidized Silicon Substrates

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Cadmium telluride (CdTe) thin-films are the most promising photovoltaic (PV) materials for lightweight and flexible solar cells because of their excellent light absorption (i.e., direct band-gap of 1.45 eV) and low-cost manufacturing processes. To improve the specific power (kW kg⁻¹) and mechanical flexibility, recent research has focused on new PV design and low-temperature (< 450 °C) deposition processes, where the active *n*-CdS/*p*-CdTe layers are directly deposited on lightweight substrates, such as polymer [1, 2] and metal foils [3]. However, the measured PV efficiencies of these low-temperature devices (< 14 %) are still far below than those fabricated using high-temperature processing methods (> 22 %). Recognizing this temperature imparity, our approach is based on high-temperature CdTe synthesis (> 450 °C) on an oxidized silicon wafer (Si/SiO₂) that can decouple the high-temperature grain growth and the subsequent thin-film lift-off / transfer processes (Figure 1). This method enables the integration of the high-quality CdS/CdTe active layers on lightweight and flexible substrates (e.g., plastic, fabric, cellulose paper) that have having the limited temperature tolerance.

In this work, we apply the post-annealing CdCl₂ treatments that are frequently used for conventional CdTe PVs fabricated on fluorine-doped tin oxide (FTO). Several previous work reported that this CdCl₂ treatments radically increase the CdTe grain size and also enhance their local optoelectronics properties. [4-6]. Prior to CdTe deposition, a thin-layer of CdS (200 nm) was evaporated at room temperature on Si/SiO₂ substrates. A 4 µm thick CdTe layer was then thermally evaporated at a fixed substrate temperature of 300 °C, 400 °C, 450 °C, and 500 °C, respectively. A portion of each sample was cleaved off and placed upside down in a graphite boat filled with CdCl₂ pellets in a tube furnace. The samples were annealed at 410 °C for 15 minutes in N₂. Figure 2 summarizes the CdTe grain size before and after the post-annealing treatments. The nominal grain size of the treated CdTe film reaches to approximately 7 µm for all samples extracted using the MIPAR software (Materials Image Processing and Automated Reconstruction) [7]. Overall, the CdTe grain size of our samples is much larger than those in conventional CdTe solar cells on glass/FTO (typical size of $\approx 1 \mu m$). The small voids near grain boundaries are noticeable with the CdCl₂ treated CdTe sample at 300 °C (Figure 2c) than in the 500 °C sample (Figure 2e). Presumably, these voids were introduced by the physical expansion of small grains (100 nm) to large ones (7 µm) during the grain recrystallization. Figure 3 shows the scanning transmission electron microscopy (STEM) and simultaneously collected energy-dispersive x-ray spectroscopy (EDX) collected by high-resolution dual detectors, confirming that highly uniform compositions of CdS and CdTe layers, closely resembling the intended configuration. Interestingly, the Te-L map reveals a distinct Te layer at the interface of CdS and SiO₂ (Figure 3d) that has not been seen in conventional CdS/CdTe PVs on FTO. We believe that the presence of this 20 nm Te-rich layer would promote the delamination of as-grown CdS/CdTe films from Si/SiO₂ substrate in water, similar to the lift-off of flexible electronics based on Ni films [8]. This Te-rich region was disappeared under the CdCl₂ treatments (Figure 3f), and it is rather uniformly redistributed in the CdS film as seen in

quantitative EDX linescans. The CdCl₂ treated samples can also be lifted-off in water like as-grown CdS/CdTe samples. The underlying physical mechanisms responsible for the delamination of as-grown and CdCl₂-treated CdS/CdTe samples are under investigation.

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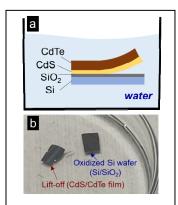


Figure 1. (a) A schematic and (b) photograph showing lift-off of CdS/CdTe film from Si/SiO₂ substrate in water.

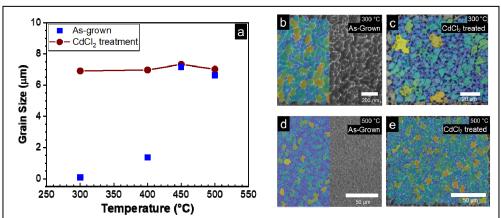


Figure 2. (a) A summary plot shows the mean values of grain size at different substrate temperatures (max of one standard deviation: $\approx 3 \mu m$). The inset shows the MIPAR processed data overlaid on an SEM image, and the statistics based on the analysis.

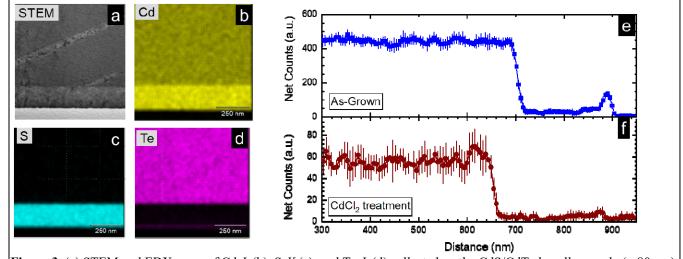


Figure 3. (a) STEM and EDX maps of Cd-L (b), S-K (c), and Te-L (d) collected on the CdS/CdTe lamella sample (≈ 80 nm). A distinct Te-rich layer (e) in the as-grown Te map disappeared after the CdCl₂ post treatments (f).