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Ka-band time-domain multiplexing front-end with minimum switch area utilization on 22 nm fully depleted silicon-on-insulator CMOS technology

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Research Paper

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Abstract

A time-domain duplexing radio frequency (RF) front-end with integrated antenna switch, power amplifier (PA), and low noise amplifier (LNA) was developed aiming for fifth-generation communication (5G) applications covering 24–28 GHz frequency range. Antenna switch utilizes pre-existing LNA input matching network together embedded with grounded shunt transistor switch to provide sufficient isolation of receive side from PA. Respectively, high impedance of off-state PA is assumed to achieve acceptable receive performance. Resulting output power is 13.6 dBm with 15 dB of peak small-signal gain at 28 GHz. Maximum average channel power was 4.8 dBm with 100 MHz 64-QAM OFDM signal within 5G adjacent channel power ratio and error vector magnitude specifications. Receive (RX) front-end achieves 5 dB noise figure at 24 GHz and 7 dB of peak gain. Performances of amplifiers degraded only by 2 dB from switch integration. The front-end dissipates 183 and 4.6 mW of power in transmit and receive mode, respectively. The simplistic design method minimizes cost both in circuit area (only 0.19 mm^2) and design time making this front-end an attractive alternative in massive phased array applications using 22 nm complementary metal oxide semiconductor (CMOS) fully depleted silicon on insulator process.

Introduction

Fifth-generation communications (5G) has started rolling out in 2019, but research has continued tirelessly to develop it further [1, 2]. Before 5G, virtually all cellular telecommunications worked sub 6 GHz and with the emergence of 5G, the frequencies have gone up to millimeter-wave (mmWave) frequencies within Ka-band using 24.25–29.5 GHz bands for example. However, mmWave frequencies pose difficulties in system design due to signal propagation issues because any obstacle attenuates signal substantially compared to sub-6 GHz frequencies [3]. Moreover, losses in integrated circuits are larger in mmWave frequencies making the problem more complex. Phased arrays are used extensively to overcome these issues with beamforming to direct radio energy between receiver and transmitter. Phased arrays, however, have to utilize multiple antennas and front-ends to reach the required effective radiated power from the transmitter which means that the performance of a single front-end is crucial for the system because the size and power dissipation are proportional to array size. Time-domain multiplexing (TDD) reduces the number of antennas in half because the same antenna is used to receive and transmit signals. This comes at a cost because a switch between the antenna, power amplifier (PA), and low noise amplifier (LNA) impacts both receive and transmit performance. Low-losses and good amplifier performance can be achieved using III–V semiconductors, however, the system cost is drastically increased in phased arrays compared to silicon-based solutions. Thanks to the scaling of CMOS technologies, the performances have been reaching III–V semiconductors and 22 nm fully depleted silicon-on-insulator (FDSOI) technology is a strong candidate for mmWave systems especially for its digital circuit capabilities together with good RF circuitry [4]. Decent output power with CMOS-SOI technologies is achieved with transistor stacking with higher supply voltages but a large signal swing can cause reliability issues in deeply scaled CMOS due to low breakdown voltages [5, 6].

Numerous TDD switches have been reported with various switch topologies. Most common switch topologies are presented in Fig. 1. Transistor-based single-pole-double-throw switches (SPDT) shown in Fig. 1(a) are compact but challenging to design with low losses higher frequencies due to parasitics. In millimeter frequencies, the parasitics are commonly resonated out with inductors but it takes area and they tend to be narrowband solutions. Another solution is to replace the series switches with quarter-wave transmission lines to isolate the amplifiers from each other (1b), but this results in larger area especially at mmWave

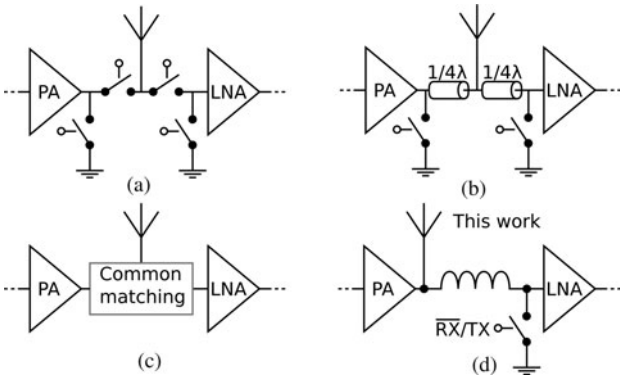

Fig. 1. Most common mmWave front-end switch topologies (a) SPDT, (b) quarter-wave transmission line SPDT, (c) common matching network, and (d) RX shunt switch.

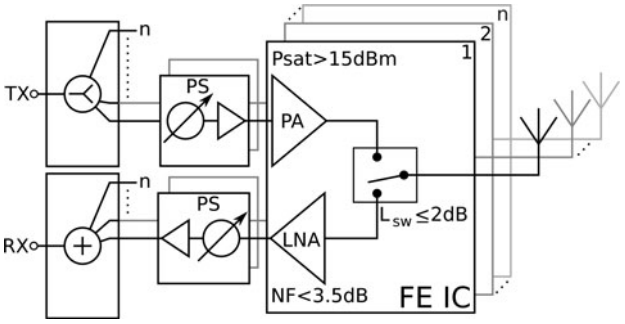

Fig. 2. Block diagram of front end as a part in a phased array system together with key system-level specifications.

frequencies where the length of the transmission line in silicon is roughly one millimeter [7]. Many types of solutions have been developed, where the matching networks for PA, LNA and antenna are shared (Fig. 1(c). In some, but not all solutions, closed-form equations have been formulated to synthesize minimum loss co-matched networks [5, 8–11]. In theory, the design is easy since only passive components need to be synthesized with a known value, but the number of matching components varies and the components might require extensive co-design in higher frequencies where losses of matching components become significant. The alternative solution proposed here is to utilize the existing LNA matching network and rely on the high impedance of off-state PA for decent performance with the minimal workload on co-designing and minimal semiconductor area resulting in low-cost solution both in silicon area and design time. Idea is shown in Fig. 1(d). Typically, LNAs have a large inductor in the input matching network to provide noise match, and this inductor is utilized together with a shunt switch much like in quarter-wavelength transmission line solutions to provide high impedance. Similar solutions have already been used by Qualcomm [12] and Liu *et al.* [13] but they use differential PAs and Liu utilizes an additional switch-inductor tank arrangement in PA output to isolate PA impedance in receive mode. We present a solution that minimizes the switch area to an absolute minimum with no additional bulky matching components.

The paper structure is as follows. In the section "System blocks", system aspects of the front-end module and the significance of switch loss are discussed. Section "3-Stack power amplifier" covers the design and measurement results of a 3-stack reference PA. Section "3-Stack power amplifier" in turn presents the same procedure for LNA. PA and LNA are then combined and integrated into a front-end in the section "Low noise amplifier" and measurement results are presented and compared to other works. The final section gives conclusions of the front-end. This paper is an extension of a paper presented at the 2020 European microwave week conference [14]. This paper gives more design details in both PA and especially on LNA. Additionally, more measurement results are presented studying the back-gate tuning of LNA and impedance levels in the front-end are studied more in-depth.

System blocks

In a phased array system, the RF front-end is the first active part that is connected to the antenna. Therefore, as modeled with Friis's system noise formula, the front-end gain and noise characteristics dominate the overall system noise. In a TDD system, antenna switch loss affects noise figure and output power directly. For example, in a 28 GHz phased array front-end developed by Rebeiz's group, antenna losses, printed circuit board (PCB) traces and front-end switch total 0.5 + 1 + 1.5 dB = 3 dB of loss which simply increases system noise figure by 3 dB and reduces output power by 3 dB, effectively limiting the link range [15]. For amplifiers, besides gain, LNA primarily has to have minimal noise. A high input compression point increases the dynamic range of the receiver and it is generally limited by amplifier stages following the LNA. Wide bandwidth enables the use of multiple frequency bands, however, widening bandwidth induces penalty in noise due to limited Q of matching components used in bandwidth extension techniques. In order to make system implementation easier, area and power dissipation should be kept low, even though power dissipation is not the major concern.

PAs, on the other hand, are major power dissipators in any communication system. PAs have to deliver high power signal with maximal efficiency. The gain of the PA dictates how much gain is needed in preceding stages and it is limited by the technology fmax and the quality of passives. As in phased arrays, total effective isotropic radiated power depends both on the individual PA output power and the number of antenna elements in the phased array. Precise specification for output power cannot be determined. But with higher output power we can either reduce the size of an array or achieve link range whichever is more desirable. Especially in integrated phased array front-ends, the output power is anyways highly limited due to the technology constraints of CMOS, CMOS SOI, and silicon germanium, and due to the large backoff required by the OFDM signal. It is preferable to minimize any losses associated with front-end. The conceptual figure of RF phased array with our front-end is shown in Fig. 2 and with the achieved system-level performances.

3-Stack power amplifier

A schematic diagram of the PA along with its micrograph is presented in Fig. 5. The PA is a 3-stack amplifier that comprises of four current combined 75 μm wide cells, totaling a 300 μm wide PA core. 3-stack allows raising the supply voltage up to 2.8 V when losses are considered and maximum $V_{ds,DC}$ of 900 mV is used. The transistor widths are the same across the stack and stepping up subsequent gate biases by 900 mV ensures that DC operating point stays identical through the stack, e.g. V_{g1} = 450 mV, $V_{g2} = 1.35\ V$ and $V_{g3} = 2.25\ V$. Each gate bias is

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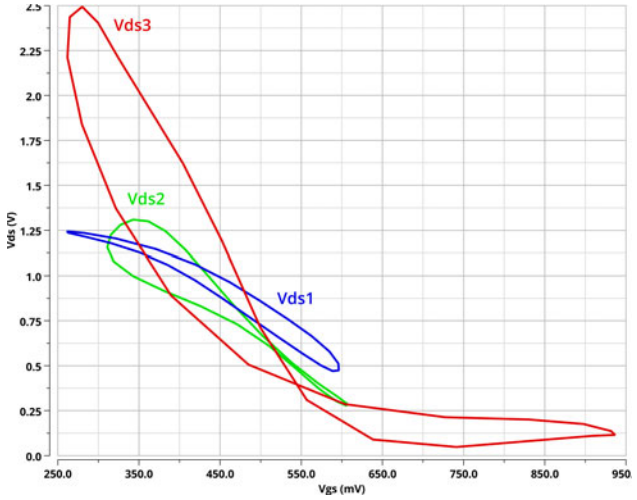

Fig. 3. Simulated 3-stack PA $V_{ds} - V_{gs}$ voltage swings at 28 GHz at 1 dB compression point.

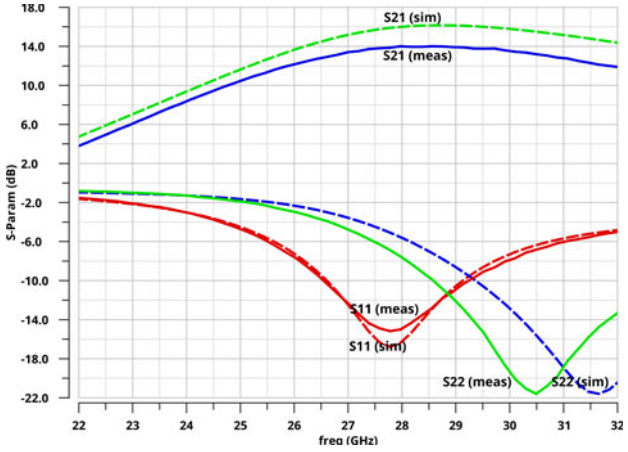

Fig. 4. Measured and simulated *S*-parameters of the stacked PA. Solid lines are measurement results and dashed lines are simulation results.

controlled via an off-chip PCB. External back-gate biasing (V_{bg1}, V_{bg2}, V_{bg3}) was enabled for all levels of the stack and were controlled in a similar manner. Signal swing is kept in phase by appropriate dimensioning of the gate capacitors C2 and C3. Voltage swings across the stack at 1 dB compression points are presented in Fig. 3 indicating a large swing over the topmost transistor. However, as reported in [16, 17], 22FDX mmW transistors can sustain quite hard overdrive. In our own 3-stack simulations (in nominal conditions), breakdown occurs when $V_{ds,DC}$ per transistor is > 1.4 *V* and $V_{ds,28\ GHz}$ > 3.9 *V*, which would mean 4.2 V of maximum VDD taking into accord supply feed DC-resistance. The gate capacitors were distributed to both sides of each power cell in order to reduce their physical size and wiring.

The PA is matched with transformers. In the input, the secondary winding of XF1 loaded with DC blocking capacitor C1 compensates the PA input capacitance and effectively changes the transformer ratio, so that conjugate matching is achieved. The simulated loss of the input matching is 4 dB. Optimum power matching impedance was determined with load-pull simulations using class AB bias (V_{g1} = 450 mV) and resulted in 7+j9 Ω for maximum output power and 6+j18 Ω for back-off. The load-pull simulations indicated that also the best PAE is achieved with these same impedances. The output matching was implemented by loading the transformer XF2 PA side winding with capacitor C4, so that the load seen by the PA is downconverted from 50 Ω. The 2.8 V supply voltage was isolated from the RF simply using a 1 nH on-chip choke. Load impedance realized by the output matching circuit is 7+j12 Ω, which is in the middle of the best high power and back-off matching. The simulated implementation loss of the output matching is 2.4 dB.

The standalone PA was verified with on-wafer measurements using Keysight N5247A (PNA-X) and Cascade Microtech 40 GHz GSG probes. The *S*-parameter measurement reference plane was at the tip of the probes.

Measured *S*-parameters with V_{g1} = 450 mV are compared with simulations in Fig. 4. As it can be seen, measured S_{11} match well with the simulations but S_{21} and S_{22} show deviation. Separately measured output matching circuit indicates that the simulated and measured output matching are in good agreement, so the difference between measured and simulated S_{22} and S_{21} may be from

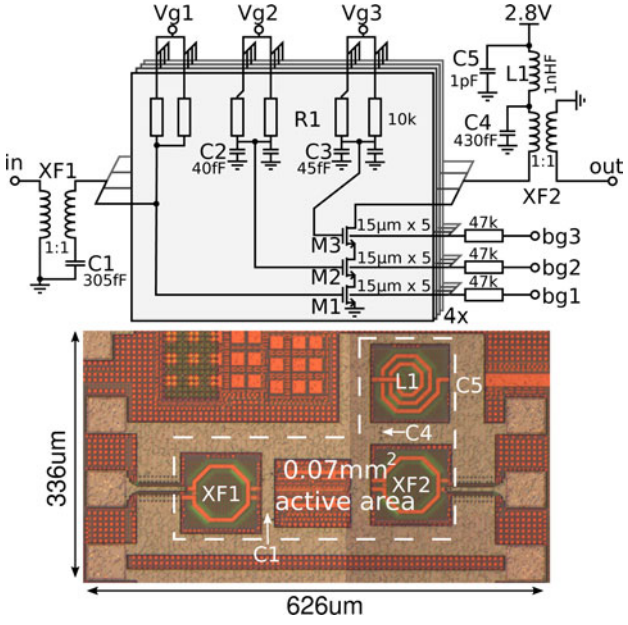

Fig. 5. Reference PA schematic diagram and micrograph.

the fact that PA core is not modeled accurately enough or due to the impact of the metal fill (metal fill grid that is visible in Fig. 5). Nevertheless, similar behavior can be seen later with LNA as well.

The key results obtained from single tone power sweep measurements are listed in Table 1. The PA has been reported in [18], but with bias setting that maximizes PAE and with pad losses removed from the results (see results "PAE bias" in Table 1). Here the main focus was to maximize gain and output power and thus completely different bias settings were used (See results "Gain bias" in Table 1).

Low noise amplifier

LNA design starts from topology choice, for mmWave frequencies, mainly two categories are used: common source and cascode topology. Common source topology has good noise and gain performance at a cost of lower isolation and stability. In turn, cascode

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Table 1. Reference PA compared to state-of-the-art Ka-band PAs

	This work							
	Gain bias	PAE bias [18]	High lin. [19]	High gain	[20]	[21]	[22]	[23]
Tech.	22 nm SOI		28 nm SOI		22 nm SOI			
Freq. [GHz]	28	28	31	31	28	27	33	28.5
Psat [dBm]	16.4	16.3	17.3	17.9	21.7	17.4	12.7	18.8
Gain [dB]	13.7	11.1	21.9	32.6	27	34	16.5	9.9
P1dB [dBm]	12.2	13.9	15.3	11.6	19.1	16.5	11.9	14.9
PAE [%]	16.7	23	24.7	25.5	27.1	19.5	40	23.4
Vdd [V]	2.8	2.8	0.7/ 1.98	0.7/ 1.98	2.4	1.2	0.9	2.8
Area [mm^2]	0.07		0.508		0.21	0.129	0.215	0.11

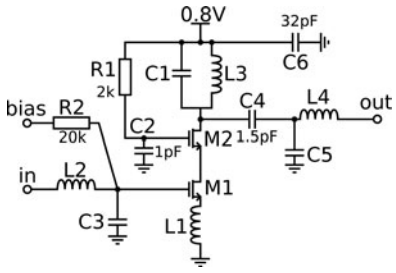

Fig. 6. Source degenerated cascode LNA schematic diagram.

Table 2. LNA cascode core transistor sweep and simulated pre-layout performance

M1,M2 width (μm)	NF	Gain	P1dB	IIP3	Lin [pH]
10	2.666	12	− 20.18	− 9.57	1477
20	2.122	13.3	− 18.02	− 7.57	943
30	2.043	13.4	− 17.23	− 6.35	763
40	2.054	13.4	− 17.06	− 5.94	600
50	2.254	13.3	− 16.76	− 5.6	572

topology has slightly worse gain and noise properties but it was chosen for its better stability. [24–27].

LNA schematic diagram is shown in Fig. 6. To match LNA simultaneously to source impedance of 50 Ω and optimum noise impedance seen by LNA input, a source degeneration inductor (L1) is used together with input matching inductor (L2) and capacitor (C3). Cascode core composes of M1 which acts as a common source gain stage followed by a common gate stage M2, which gate is ac-grounded with C2. The output is loaded with a parallel LC-resonant tank (C1 and L3) for desired center frequency and output is matched to 50 Ω with L4 and C5. C4 is a DC-block capacitor allowing easy integration of possible future second stage. The DC-block capacitor is omitted from the input to minimize input losses that have a large impact on noise figure since mmWave antennas are typically patch antennas with no DC-path to ground.

The design of the LNA starts from choosing values for L1, L3, and transistor widths. 70 pH was chosen for degeneration inductor together with 120 pH for load inductor to have provided stable gain. A higher ratio of L3 to L1 results in higher gain at a cost of stability. Next, core is biased to conduct 150 μA/ μm for optimum noise performance. Then load resonator is tuned to correct frequency with C1 after which noise and gain circles can be simulated to determine values for input matching network components. Lastly, the output matching network is dimensioned and LNA is characterized. This design procedure was repeated for multiple transistor widths to find an optimum width using a schematic model of the LNA using design kit capacitor models, pre-layout estimates of transistor parasitics and using a finite Q of 18 for all inductors. Table 2 shows a sweep of transistor size and simulated performance. As transistor width is increased, linearity improves and input matching inductor size reduces. 30 μm was chosen for optimal noise and gain performance. Simulations of designed LNA predict stable behavior from stability factors K, μ, and Δ which are all within stable values ($K > 1$, $\mu > 1$, and $\Delta > 0$).

A micrograph of manufactured LNA is shown in Fig. 7. Matching inductor values were adjusted to compensate for added parasitic inductances from pads input feed, core input and ground return path. To support front-end integration, C3 (8fF) was replaced with a shunt switch (M3) of equal capacitance with negligible impact on performance. To check robustness for the front-end environment, a simulation was done feeding power to LNA input and a parallel 50 Ω load modeling an antenna. At 28 GHz the switch can withstand 18 dBm of PA power holding voltage swings below 0.8 V. Lastly, connections were routed out from LNA core from the back-gates of the transistors in order to study possible performance enhancements possibilities. In this process, transistors have the back-gate option, which allows threshold voltage tuning with roughly 80 mV/V sensitivity.

On-wafer measurements for S-parameters and 1-tone compression were conducted using Keysight N5247A (PNA-X) with Cascade Microtech 40 GHz GSG probes. Noise figure was measured with noise source 346CK01, preamplifier U7228F and UXA signal analyzer N9040B with noise figure option (all Keysight equipment). Back-gate effects were studied by sweeping back-gates of amplifier transistors one by one while keeping bias current constant with the front gate of M1. Cascode transistor back-gate sweep is shown in Fig. 8(a). We observe improvement in gain (0.15 dB), linearity (1 dB) and noise figure (0.11 dB) when back-gate voltage is increased from 0 to 2 V. This is because

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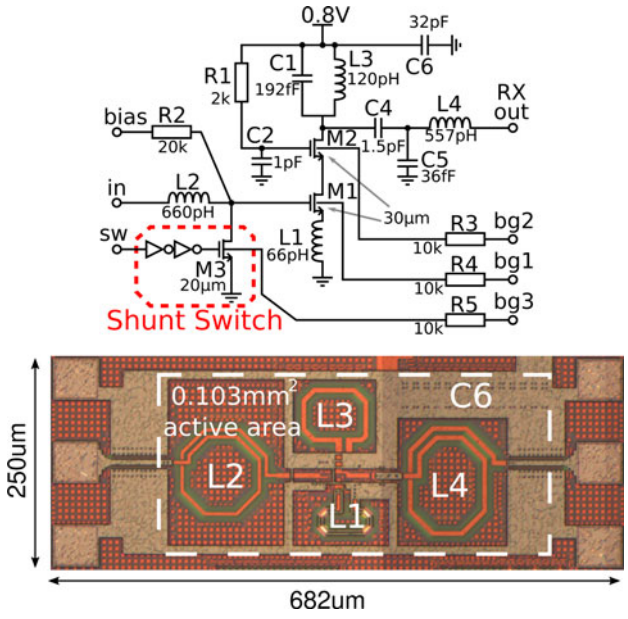

Fig. 7. Reference LNA schematic diagram and micrograph.

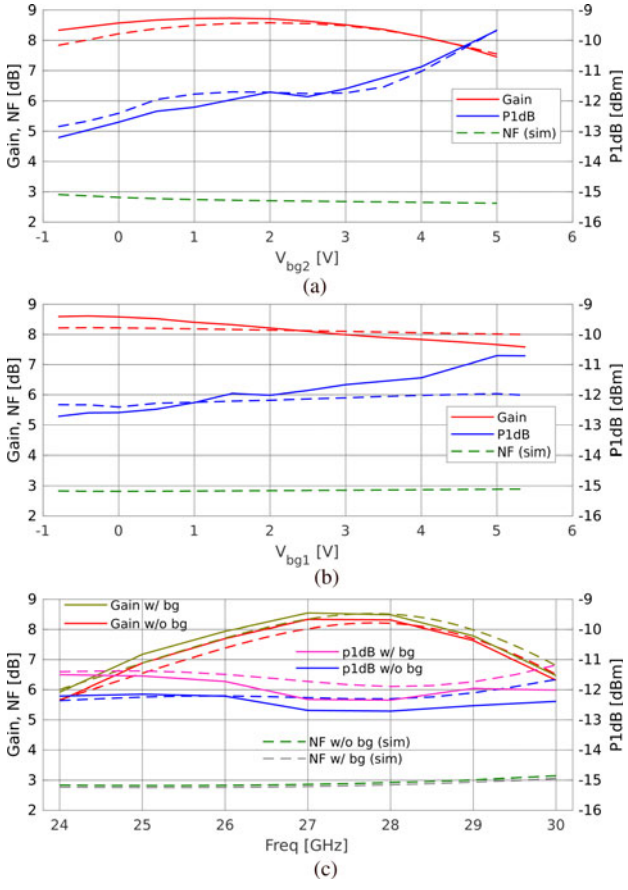

Fig. 8. Reference LNA back-gate experiments with constant bias current of 0.19 mA/µm adjusted with front-gate bias. (a) Cascode back-gate sweep, (b) Input transistor back-gate sweep and c) Optimum back-gate bias setup of $V_{bg1} = -0.4$ V, ~ $V_{bg2} = 0.9$ V, $V_{bias} = 0.5$ Vcompared to 0 V back-gates and $V_{bias} = 0.475$ V. Solid plots are measurement results and dashed are acquired from simulations.

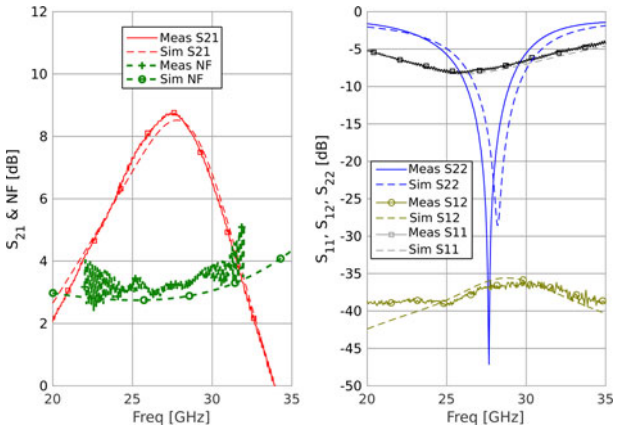

Fig. 9. Reference LNA measured and simulated *S*-parameters and noise figure.

the voltage drop is being equalized between the two transistors meaning there is more gain and more headroom in the output signal swing. Above 2 V, the voltage drops over M1 and M2 go off-balance resulting in a greatly degrading gain. Sweeping the input transistor (Fig. 8(b), back-gate does not show much changes, the optimum gain point is with negative back-gate voltage with a small cost of linearity. Gain-wise optimum bias setup was found to be of $V_{bg1} = -0.4$ V, $V_{bg2} = 0.9$ V, and $V_{bias} = 0.5$ V which consumes 5.7 mA with 0.8 V supply or 190 $\mu A/\mu m$ of bias current. Gain optimum bias setup is compared to bias setup with no back-gates (backgates at 0V) in Fig. 8(c). At peak gain frequency, gain is improved by 0.2 dB, compression point by 0.36 dB and noise (from simulations) 0.07 dB. S-parameter results of this optimum gain bias setup is presented in Fig. 9 showing 8.7 dB of gain and 3 dB of noise figure. The circuit was modeled with parasitics extractor tool up to highest digital routing metal layer and thick metals were EM-modeled using Keysight Momentum. Measurements and simulations have good agreement with only a small discrepancy in output matching capacitor and load resonator capacitor capacitances. Lower gain and noise performance (3 dB) from initial simulations (Table 2) arise from parasitics of transistor core and lower *Q*-figures (about 15) for inductors.

LNA is compared to other state-of-the-art Ka-band LNAs in Table 3. State-of-the-art LNAs have better gain and noise behavior but at cost of power dissipation. Reported references mostly utilize higher than nominal supply voltages to improve gain, noise and linearity, whereas we used nominal 0.8 V supply for easier integration for possible future systems (no need for an additional supply voltage for the chip).

Front-end

Combining LNA and FE into a front-end requires a few changes from reference amplifiers and results in the minimal additional area as we can see from Fig. 10 front-end micrograph. First, the output of PA and input of LNA have to be shifted by 90° to combine the nets into one. Second, LNA bias needs to be prevented from leaking to PA output matching ground by adding a DC-block, which in this case was put in PA output transformer (C6 in Fig. 10) as it did not take any additional area and its impact on TX and RX performance is insignificant as its value is high. Due to the changed impedance environment for both LNA and PA, their matching networks had to be slightly adjusted. LNA input inductor (L2) had to be increased from 660 to 710 pH to

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Table 3. Reference LNA compared to state-of-the-art Ka-band CMOS LNAs

Ref	This Work	[24]	[24]	[25]	[26]	[27]
Topology	Casc.	Casc.	2-st. CS	CS+ Casc.	Casc.	Casc.
Freq. [GHz]	23.3–30.5	21.6–32.8	19.5–29	22–32	19–34	14–31
Gain [dB]	8.7	7.8	16.9	20.1	12	12.8
NF [dB]	3	2.65	2.18	1.73	1.46	1.4
Supply [V]	0.8	0.8	0.4	0.42/ 1.05	1.3	1.5
Pdiss [mW]	4.6	6	3.2	17.2	9.8	15
Tech.	22 nm SOI	22 nm SOI	22 nm SOI	22 nm SOI	22 nm SOI	45 nm SOI

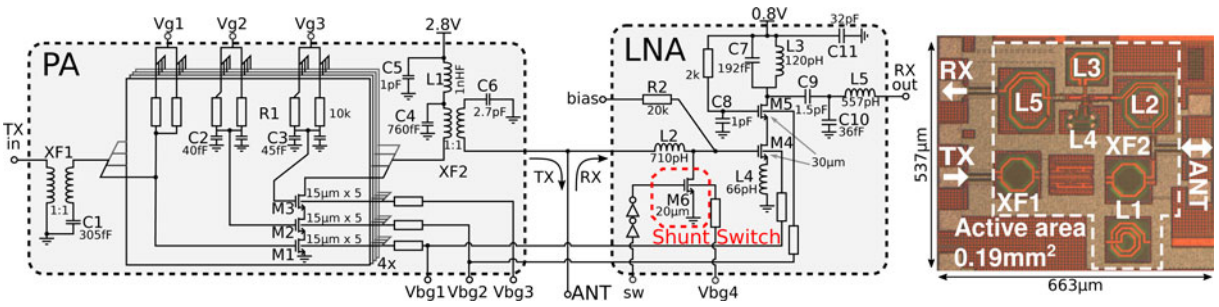

Fig. 10. Front-end schematic diagram and micrograph.

optimize noise match and in turn, PA output was compensated with C4 increase from 430 to 760 fF. Capacitance increase compensates the PA gain loss from LNA addition at a small cost of efficiency and saturated output power level. The robustness of the switch was again tested in the simulator by driving the PA at saturated power and checking voltage swings over the switch while sweeping antenna impedance in the Smith chart. Voltage swings stayed well within 0.8 V up to 1:8 of VSWR.

To study how the impedance environment changes due to front-end integration, matches for both amplifiers were analyzed from *S*-parameter measurements and simulations. For minimum switch loss, both amplifiers would have to appear as 0 dB matches for each other in respective transmit and receive modes. Changes in impedance levels for reference amplifiers at antenna port are illustrated in Figs 11 and 12. For these figures, input feeds were de-embedded from measurement results using on-chip reflect impedance standards. In front-end simulations, the feeds were removed and the connection to the loading amplifier side was cut to model the front-end environment more accurately when looking directly at LNA input and PA output. For LNA, we get a quite good increase of impedance levels (−5.5 to −2 dB) due to large input inductor and grounding shunt switch. However, hand calculation with 25 Ω switch resistance and 710 pH L2 predict nearly 1 dB higher match:

$$Z_{rx} \approx j2\pi fL_2 + Z_{sw} = 25 + j124.9\Omega \quad (1)$$

$$S_{11} = -20 \cdot log_{10}(|\Gamma|) \quad (2)$$

$$S_{11} = -20 \cdot log_{10}\left(\left|\frac{Z_{rx} - Z_0}{Z_{rx} + Z_0}\right|\right) = -1.17\,\text{dB} \quad (3)$$

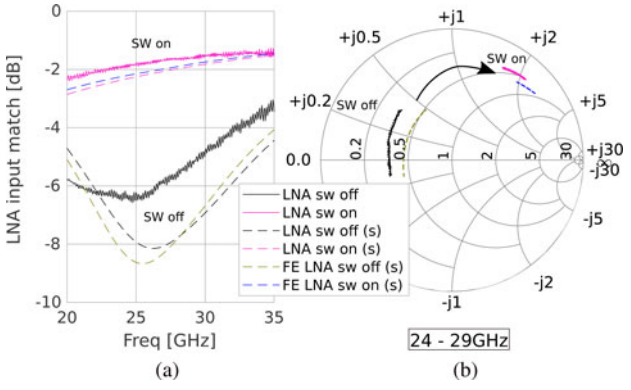

Fig. 11. Input matches of reference LNA (measured) and front-end LNA (simulated) with switch in receive mode (SW OFF), and in transmit mode (SW ON) in dB scale (a) and in Smith chart (b).

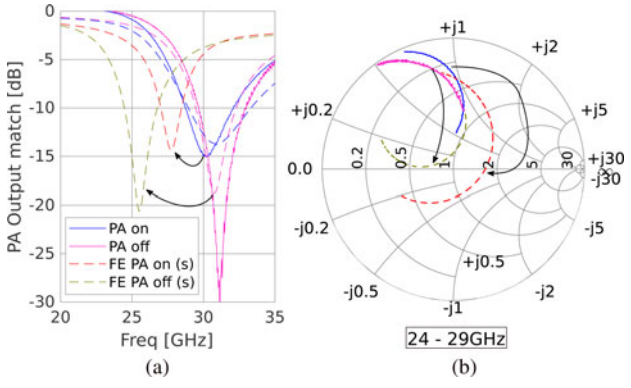

Fig. 12. Output matches of reference PA (measured) and front-end PA (simulated) in on and off state in dB scale (a) and in Smith chart (b). Arrows illustrate the changes from PA to FE PA.

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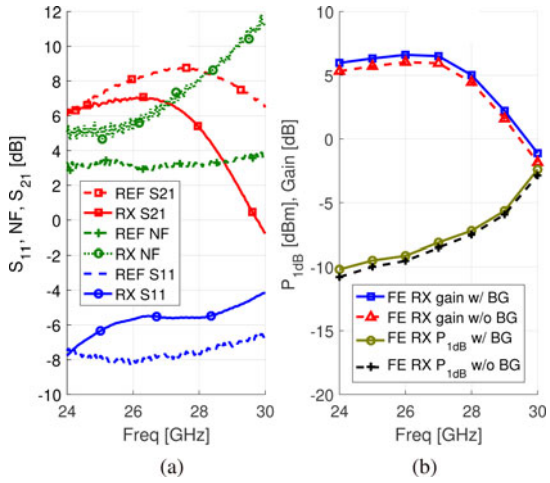

Fig. 13. RX *S*-parameter (a) and 1-tone measurement (b) results. *S*-parameter results are in optimum gain bias setup and zero back-gate bias compression point and gain are compared in right plot.

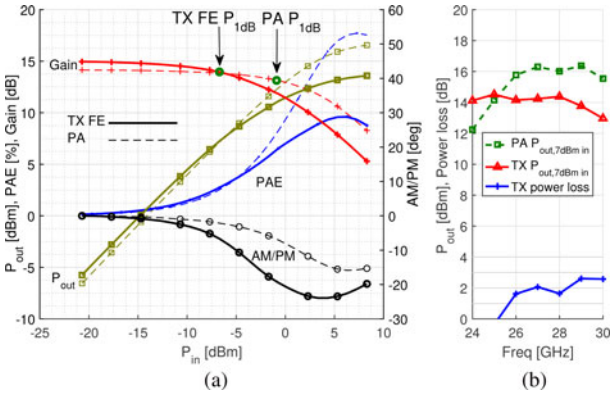

Fig. 14. Measured PA and TX 1-tone responses at 28 GHz (left) and saturated power comparison.

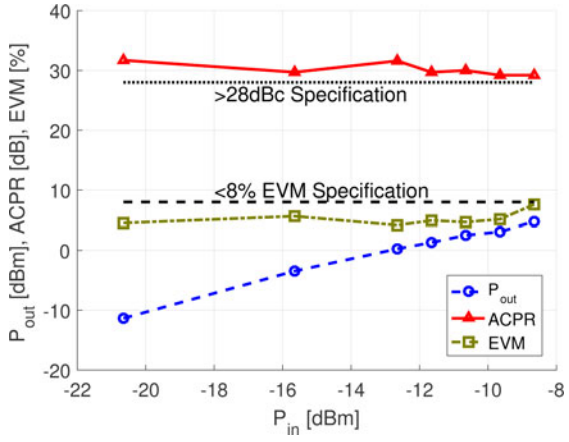

Fig. 15. ACPR and EVM of TX with swept input power with 100 MHz 64-QAM signal at 28 GHz. 5G specifications for ACPR and EVM are highlighted. Input and output powers are reported as channel average power.

Difference in matching between theory and practice potentially comes from limited Q of the inductor and its parasitic capacitances. PA output match in front-end turned out to be worse upon integration. Switching PA off improves impedance levels in LNA point of view only by small amount, however, turning PA completely off eliminates any noise it generates since there is only little isolation from PA core to LNA input.

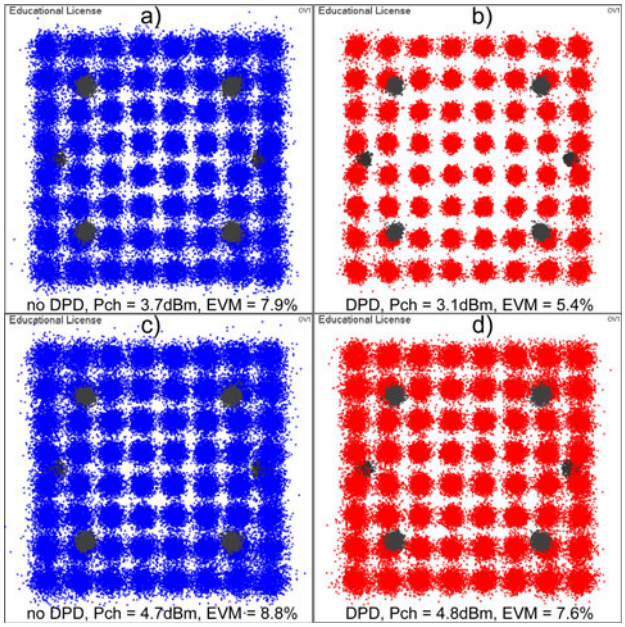

Fig. 16. Measured constellations of TX with maximum in-specification power (bottom) and with 1 dB lower input power. Left constellations are without DPD and right constellations are with DPD.

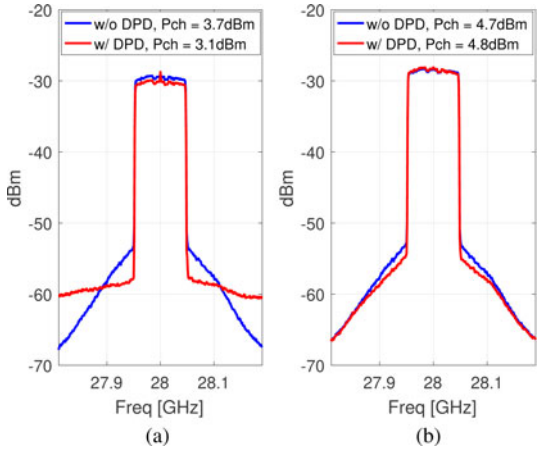

Fig. 17. Output spectrum of TX with and without DPD. (a) is with input power 1 dB below maximum in-specification power and (b) is with maximum in-specification output power.

RX measurements

Measurement results for receive side are shown in Fig. 13. Due to leakage of signal to TX side, the LNA gain and noise figure have degraded about 2 dB below 26 GHz and due to resonance in TX side, gain and noise figure degrade rapidly above 28 GHz. Fig. 13(b) shows that back-gate study from LNA measurements apply also for front-end RX. Optimum back-gate settings improve gain and compression point. RX is providing peak gain of 7 dB with minimum NF of 5 dB with input compression point of −9.1 dBm.

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Table 4. Comparison of mmWave TDD front-ends. Reported frequency range is 3 dB bandwidth

	RX shunt gate			SPDT			1/4λ TL	Common matching				
SW type Ref.	This work	ISSCC 2018 [12]	RFIC 2020 [13]	TMTT 2016 [28]	JSSC 2018 [15]	TMTT 2020 [29]	JSSC 2017 [7]	MWCL 2016 [8]	JSSC 2020 [9]	ESSCIRC 2017 [10]	TMTT 2019 [5]	RFIC 2020 [11]
Freq [GHz]	24–28	25–30.5	25.5–29.5	30–40	27.8–32.2	22.7–40	27–29	57–65	27–40	60–67	25–30	24–28
FE LNA topology	Casc.	–	Casc.	Casc.	CS	diff. Casc.	CS	Casc.	diff. CG	diff. CG	Casc.	diff. CS
RX peak gain [dB]	7	34[a]	15.6	17	20	19.3	30[a]	21.5	16.1	17	11	23.2
RX P1dB [dBm]	− 9.1	–	− 15.8	− 17	− 22	− 16	− 22.5	–	− 15.7	− 25	− 7.1	− 9
RX NF [dB]	5–8	3.8–4.4[a]	2.8–3.6	7.9–8.4 (sim)	4.5–5	4	6	6.7–9.1	6.2–8.3	7.6–9.8	3.2–3.8	4.4–6.8
RX Pdiss [mW]	4.6	42[a]	30.7	48	130	36	103.1[a]	39.6	17.6	<28.8	28	40
FE PA topology	3-stack	diff. CS	3-stack	4-stack	diff. 2-stack	3-stack	2-stack	2-stack	diff. CS	diff. CS	4-stack	diff. CS
TX peak gain [dB]	15	44[a]	30	14	20	17.6	15	24.5	28.5	24	12	28
TX P1 dB [dBm]	7.4	12[a]	16	20.5	10.5	18.3	13.5	5	14.1	10	22	16.1
TX Pdiss [mW]	184	90[a]	185[b]	352	200[c]	370	143.8[a]	71	96.2	<63.5	230	310[b]
Psat [dBm]	13.6	14	17.2	22.5	12.5	19.1	16	8.4	15.8	10	23.6	18.2
pPAE [%]	9.6	20	21.5	7	13[c]	18	21	8.7	20	–	28	21.1
Active area [mm2]	0.19	1.16[a]	0.17	7[a]	2.16[d]	1.05	4	0.22	0.35	0.35	0.275	0.94
Tech.	22 nm	28 nm	22 nm	130 nm SiGe	180 nm SiGe	45 nm	130 nm SiGe	65 nm		28 nm	45 nm	65 nm

[a]complete TX/RX chain.
[b]estimated from pPAE,P1 dB and gain.
[c]at P1 dB.
[d]estimated from micrograph.

TX measurements

TX 1-tone measurements show degradation due to switch arrangement compared to reference PA. Measurement results at 28 GHz in Fig. 14(a) indicates that the switch lowers compression point by about 5 dB and saturated output power by only 2 dB. Non-linear load caused by the switch transistor M6 and LNA also results in an impact on AM/PM behavior with respect to the reference PA but only by a few degrees. Modification to matching capacitor C4 and parallel RX side has also changed the output center frequency from 28 to 26 GHz and bandwidth extension is observed due to de-Q of PA output matching environment in Fig. 14(b). Resulting gain, 1 dB compression point and saturated output power at 28 GHz are 15 dB, 7.4 dBm and 13.6 dBm, respectively.

To study the linearity of the front-end in realistic 5G application, modulated signal measurements were carried out using 100 MHz wide cyclic prefix – orthogonal frequency division multiplexing (CP-OFDM) 64-QAM modulated signal following the 3GPP/NR standard for FR2 frequency band. 5G specifications for FR2 band limit adjacent channel power ratio (ACPR) to −28 dBc and error vector magnitude (EVM) to 8% [30]. To maximize channel power, digital predistortion (DPD) was used for the modulated signal. The signal was generated with Keysight M8190A Arbitrary waveform generator and then up-converted to 28 GHz by Keysight E8267E signal generator. The output of the front-end was then measured with Keysight N9040B UXA which analysed the ACPR and EVM. ACPR and EVM measurements are shown in Fig. 15. Resulting specification limited maximum channel power was measured to be 4.8 dBm which is close to 9 dB maximum practical back-off from saturated output power for the 64-QAM OFDM signal so all available output power is possible to utilize with the DPD. EVM of 7.6% leaves about 2.5% (−32 dBV) for rest of the transmitter chain, such as local oscillator phase noise, I/Q imbalance, thermal noise and data converter non-idealities, which is challenging but doable task to implement at mmWave frequencies.

Constellation diagrams and spectrums for maximum achievable channel power and 1 dB below maximum power are shown in Figs 16 and 17. Despite degraded linearity from front-end integration, the front-end meets the EVM specification without DPD with only 1 dB lower signal power (Fig. 16(a) however ACPR remains as a bottleneck.

Comparison and discussion

The front-end key performance metrics are shown and compared to other Ka-band front-ends in Table 4. Simple switch technique results among the most compact front-end designs with comparable output power, efficiency and noise performance with exceptionally low RX power dissipation. Cascode is clearly the most popular LNA topology. Even though some front-ends have common source LNA, it is difficult to distinguish the topology from performance due to various switch techniques, number of stages and technology. That can not be said on PA topologies where the common trend is a couple dB power increase per increased stack number. Our design, unfortunately, suffers from lower output power due to switch non-linearity and gain preferred PA matching. Simulations show that reverting back to reference PA value for C4 and boosting PA VDD up to 3.5 V would regain reference PA compression point but with large power dissipation of 456 mW and reliability risks related to high VDD. Theoretical 3dB increase in signal power due to differential structures is evident from comparable output power of differential CS stages (1-stack) but at the cost of power and area.

On basis of measurement results, it is evident that performance is good below 26 GHz (see flat NF behavior in Fig. 13(a). So the designing of higher center frequencies of individual amplifiers might be beneficial so the lower frequency band can be utilized more readily. Additionally, instead of preferring gain, front-end PA matching should be done in more favor of power, and then compensating the lost gain with pre-driver PAs. In this way, the PA output impedance is potentially higher resulting in better isolation to the RX side. To combat the low TX compression point, M6 switch width could be increased but the increase of off-state capacitance would degrade LNA noise matching in RX-mode. Also reducing the widths of LNA transistors would result in a larger gate inductor (see Table 2) resulting in better isolation of RX side from TX, again with some noise penalty, while optimizing inductor Q.

Conclusion

We have presented a minimum area solution for a Ka-band TDD PA, LNA and switch front-end utilizing LNA matching network with shunt switch. Front-end switch performance was evaluated by comparing front-end performance to standalone reference amplifiers presented in this paper. TX provides 13.6 dBm of saturated output power at 28 GHz proving only 2 dB loss in output power and 4.8 dBm of channel power with 5G NR FR2 100 MHz wide OFDM signal with 9 dB backoff. At 24 GHz, the receive noise figure is 5 dB and gain 7 dB which are only 2 dB lower than of reference LNA relying on high impedance of an off-state PA. The paper also presents measurement and simulation results of back-gate option in used 22 nm FDSOI technology for LNA to improve gain and linearity. Possible improvements are discussed to decrease switch arrangement losses on overall performance. Active area (0.19 mm^2) and first stage LNA power dissipation (4.6 mW) of the front-end is among the smallest reported to the author's best knowledge.

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References

1. **(2020) IET, 6G and the reinvention of mobile:** 5G networks have scarcely started to roll out, yet experts believe we'll need 6 G to keep up with the super-smart apps of the 2030s. *Engineering & Technology* **1**, 26–29.
2. **Shafi M, Tataria H, Molisch AF, Tufvesson F and Tunnicliffe G** (2020) Real-time deployment aspects of C-Band and millimeter-Wave 5G-NR systems. *IEEE International Conference on Communications (ICC)*, Dublin, Ireland.
3. **Rappaport TS, Xing Y, MacCartney GR, Molisch AF, Mellios E and Zhang J** (2017) Overview of millimeter wave communications for fifth-generation (5G) wireless networks? With a focus on propagation models. *IEEE Transactions on Antennas and Propagation* **12**, 6213–6230.
4. **Ong SN, Lehmann WH, Chow WH, Zhang C, Schippel C, Chan LHK, Andee Y, Hauschildt M, Tan KKS, Watts J, Lim CK, Divay A, Wong JS, Zhao Z, Govindarajan M, Schwan C, Huschka A, Bcllaouar A, LOo W, Mazurier J, Grass C, Taylor R, Chew KWJ, Embabi S, Workman G, Pakfar A, Morvan S, Sundaram K, Lau MT, Rice B and Harame D** (2018) A 22 nm FDSOI technology optimized for RF/mmWave applications. *Proceedings of Radio Frequency Integrated Circuits (RFIC)*, Philadelphia, PA, USA.

https://doi.org/10.1017/S1759078721000428 Published online by Cambridge University Press

5. **Rostomyan N, Özen M and Asbeck PM** (2019) Synthesis technique for low-loss mm-Wave T/R combiners for TDD front-ends'. *IEEE Transactions on Microwave Theory and Techniques* **3**, 1030–1038.
6. **El-Aassar O and Rebeiz GM** (2019) 4.7 A compact DC-to-108 GHz stacked-SOI distributed PA/Driver using multi-drive inter-stack coupling, achieving 1.525 THz GBW, 20.8 dBm peak P1 dB, and over 100 Gb/s in 64-QAM and PAM-4 modulation, ISSCC, San Francisco, CA, USA.
7. **Sadhu B, Tousi Y, Hallin J, Sahl S, Reynolds SK, Renström Ö, Sjögren K, Haapalahti O, Mazor N, Bokinge B, Carlinger A, Westesson E, Thillberg JE, Rexberg L, Yeck M, Gu X, Ferriss M, Liu D, Friedman D and Valdes-Garcia A** (2017) A 28-GHz 32-Element TRX Phased-Array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications. *IEEE Journal of Solid-State Circuits* **12**, 3373–3391.
8. **Meng F, Ma K, Yeo KS, Boon CC, Yi X, Sun J, Feng G and Xu S** (2016) A Compact 57–67 GHz bidirectional LNAPA in 65-nm CMOS technology. *IEEE Microwave and Wireless Components Letters* **8**, 628–630.
9. **Mondal S and Paramesh J** (2020) Power-efficient design techniques for mm-Wave Hybrid/Digital FDD/Full-Duplex MIMO transceivers. *IEEE Journal of Solid-State Circuits* **8**, 2011–2026.
10. **Khalaf K, Vaesen K, Brebels S, Mangraviti G, Libois M, Soens C and Wambacq P** (2017) A 60 GHz 8-way phased array front-end with TR switching and calibration-free beamsteering in 28 nm CMOS, ESSCIRC, Leuven.
11. **Zhu W, Wang J, Lv W, Zhang X, Liao B, Zhu Y and Wang Y** (2020) A 24–28 GHz Power and Area Efficient 4-Element Phased-Array Transceiver Front-End with 21.1% /16.6% Transmitter Peak/OP1dB PAE Supporting 2.4 Gb/s in 256-QAM for 5-G Communications, RFIC, Los Angeles, CA, USA.
12. **Dunworth JD, Homayoun A, Ku B-H, Ou Y-C, Chakraborty K, Liu G, Segoria T, Lerdworatawee J, Park JW, Park HC, Hedayati H, Lu D, Monat P, Douglas K and Aparin V** (2018) A 28GHz Bulk-CMOS dual-polarization phased-array transceiver with 24 channels for 5G user and basestation equipment, ISSCC, San Francisco, CA, USA.
13. **Liu Y, Tang X, Mangraviti G, Khalaf K, Zhang Y, Wu WM, Chen SH, Bebaillie B and Wambacq P** (2020) A 28 GHz front-end module with T/R switch achieving 17.2 dBm Psat, 21.5% PAEmax and 3.2 dB NF in 22 nm FD-SOI for 5G communication, RFIC, Los Angeles, CA, USA.
14. **Hietanen M, Rusanen J, Aikio JP, Tervo N, Rahkonen T and Pärssinen A** (2021) Ka-Band TDD front-end with gate shunt switched cascode LNA and three-stack PA on 22 nm FDSOI CMOS technology. *2020 50th European Microwave Conference (EuMC)*, Utrecht, Netherlands, 945–948.
15. **Kibaroglu K, Sayginer M and Rebeiz GM** (2018) A low-cost scalable 32-Element 28-GHz phased array transceiver for 5G communication links based on a 2×2 beamformer flip-chip unit cell. *IEEE Journal of Solid-State Circuits* **5**, 1260–1274.
16. **Chen T, Zhang C, Arfaoui W, Bellaouar A, Embabi S, Bossu G, Siddabathula M, Chew KWJ, Ong SN, Mantravadi M, Barnett K, Taylor R and Janardhanan S** (2019) Excellent 22FDX hot-carrier reliability for PA applications. *Proceedings of Radio Frequency Integrated Circuits (RFIC) Symposium*, Boston, MA, USA.
17. **Arfaoui W, Bossu G, Muhlhoff A, Lipp D, Manuwald R, Chen T, Nigam T and Siddabathula M** (2020) A novel HCI reliability model for RF/mmWave applications in FDSOI technology. *2020 IEEE International Reliability Physics Symposium (IRPS)*, Dallas, TX, USA.
18. **Rusanen J, Hietanen M, Sethi A, Rahkonen T, Pärssinen A and Aikio JP** (2019) Ka-Band stacked power amplifier on 22 nm CMOS FDSOI technology utilizing back-gate bias for linearity improvement. *IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)*, Helsinki, Finland.
19. **Torres F, Kerhervé E, Cathelin A and De Matos M** (2021) A 31 GHz body-biased configurable power amplifier in 28 nm FD-SOI CMOS for 5 G applications. *International Journal of Microwave and Wireless Technologies* **13**, 3–20.
20. **Zong ZSEP, Tang X., Nguyen J, Khalaf K, Mangraviti G., Liu Y and Wambacq P** (2020) A 28 GHz two-way current Ccombining stacked-FET power amplifier in 22 nm FD-SOI. *IEEE Custom Integrated Circuits Conference (CICC)*, Boston, MA, USA.
21. **Elgaard C, Aderson S, Caputa P, Westesson E and Sjöand H** (2019) A 27 GHz adaptive bias variable gain power amplifier and T/R switch in 22 nm FD-SOI CMOS for 5G antenna arrays. *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Boston, MA, USA.
22. **Abdulaziz M, Hünerli HV, Buisman K and Fager C** (2019) Improvement of AM-PM in a 33-GHz CMOS SOI Power amplifier using pMOS neutralization. *IEEE Microwave and Wireless Components Letters* **29**, 798–801.
23. **Aikio JP, Hietanen M, Tervo N, Rahkonen T and Pärssinen A** (2019) Ka-Band 3-Stack power amplifier with 18.8 dBm Psat and 23.4% PAE using 22 nm CMOS FDSOI technology. *IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, Orlando, FL, USA.
24. **El-Aassar O and Rebeiz GM** (2020) Design of low-power Sub-2.4dB mean NF 5G LNAs using forward body bias in 22 nm FDSOI. *IEEE Transactions on Microwave Theory and Techniques* **10**, 4445–4454.
25. **Cui B, Long JR and Harame DL** (2019) A 1.7-dB Minimum NF, 22–32 GHz Low-Noise Feedback Amplifier with Multistage Noise Matching in 22-nm SOI-CMOS, RFIC, Boston, MA, USA.
26. **Zhang C, Zhang F, Syed S, Otto M and Bellaouar A** (2019) A Low Noise Figure 28 GHz LNA in 22 nm FDSOI Technology, RFIC, Boston, MA, USA.
27. **Li C, El-Aassar O, Kumar A, Boenke M and Rebeiz GM** (2018) LNA Design with CMOS SOI Process-l.4dB NF K/Ka band LNA, IMS, Philadelphia, PA.
28. **Liu C, Li Q, Li Y, Deng X, Tang H, Wang R, Liu H and Xiong WZ** (2016) A Ka-Band single-chip SiGe BiCMOS phased-array transmit/receive front-end. *IEEE Transactions on Microwave Theory and Techniques* **11**, 3667–3677.
29. **Lokhandwala M, Gao L and Rebeiz GM** (2020) A high-power 24–40-GHz transmit-receive front end for phased arrays in 45-nm CMOS SOI. *IEEE Transactions on Microwave Theory and Techniques*.
30. **3GPP, Base Station (BS) radio transmission and reception,** 3rd Generation Partnership Project (3GPP), Technical Specification (TS) 38.104, October 2019, version 16.1.0 [Online]. Available at https://www.3gpp.org/ftp/Specs/archive/38_series/38.104/38104-g10.zip.

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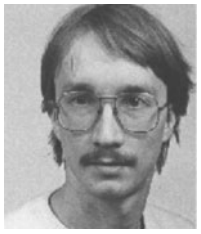

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