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Towards Mapping Electrostatic Potentials in Semiconductor Devices Under Working Conditions Using Off-Axis Electron Holography

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The electrical performance of a semiconductor device relies strongly on how precisely the electrostatic potentials are distributed across the active region. An accurate measurement of this potential distribution is of vital interest to the semiconductor industry, particularly if it can be carried out under actual device operating conditions. The technique of off-axis electron holography in the transmission electron microscope (TEM) is a promising candidate for fulfilling the required accuracy in mapping electrostatic potentials. Here, we present electron holography measurements from an actual *n*-type metal-oxide-semiconductor field-effect-transistor (NMOSFET) under electrical biasing conditions.

A TEM lamella was prepared from an array of Si NMOSFETs buried under layers of metallization and oxidation using focused ion beam (FIB) milling. Most of these layers were removed using FIB milling to reach the source/drain W plugs. Also, part of the *p*-type substrate was removed and a W line was deposited in the FIB workstation for making the electrical contact to the substrate (Fig.1a). In order to avoid curtaining effects during FIB milling, all of the thinning and low voltage polishing steps were carried out from the substrate side. The crystalline thickness of the specimen was measured to be 470±10 nm. The prepared specimen was electrically biased using a TEM holder with two fixed electrical contacts, which were connected to the W line, as well as one sharp nano-positionable Au needle, which was used for making the electrical contact to the source/drain. The diode current-voltage characteristic (Fig. 1b) measured from the *pn* junction between the source/drain and substrate proves that the transistors are not damaged significantly during specimen preparation and can be considered as working devices.

Holograms (with an overlap width of 650 nm and a fringe spacing of 3 nm) were acquired using an FEI Titan 80-300 TEM operated at 120 kV. The phase images shown in Fig. 2 are from transistor T_1 (marked in Fig. 1a) for a range of forward and reverse voltages applied between the source/drain region under the W_1 plug and the *p*-type substrate. It can be seen that, in response to the increase and decrease of the potential across the n^+-type source/drain and *p*-type substrate, under reverse and forward bias conditions the phase change increases and decreases correspondingly. The line profiles obtained from under the gate, along arrow A marked in Fig 2.d for different biasing voltages, are shown in Fig. 3a. These profiles show that the electrostatic potential of the source, which is electrically biased, increases and decreases with reverse and forward voltage, respectively, while the electrostatic potential of the unbiased drain remains almost unchanged relative to the vacuum level. In this biasing configuration, the two other terminals of the transistor, the gate (G) and the other W plug (W_2), are electrically floating and may acquire a voltage during the experiment. However, the phase profiles from the oxide region above the gate between the two W plugs, shown in Fig. 3b, suggest that the potential of the unbiased W_2 plug

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remains almost unchanged. The slope of these phase profiles represents the electric field in the oxide region. As shown in Fig. 3c, this electric field increases linearly with the biasing voltage applied to the W_1 plug. From Fig. 3a, it can also be deduced that the gate voltage is approximately half of the bias voltage, because the phase increases linearly between the two W plugs. The gate is placed approximately half-way between the two W plugs. Therefore, the linear and continuous increase in the phase profile above the gate between the two plugs shows that the potential difference is the same between the gate and each plug. Although, in this way, the voltage of all four terminals of the transistor (source, drain, gate and substrate) can be estimated, accurate extraction of the potential map will require electrical contacts to all four terminals in a future experiment. The effects of the electron beam, FIB damage and external fringing field also need to be assessed. Nevertheless, this experiment suggests that the *in-situ* examination of semiconductor devices under working conditions in the TEM is a realistic perspective [1].

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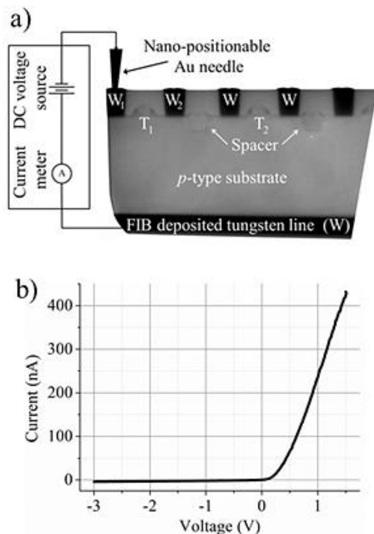

Figure 1.a) Schematic diagram showing how an electrical bias was applied to an NMOSFET. b) A typical IV curve measured from the biasing configuration in a).

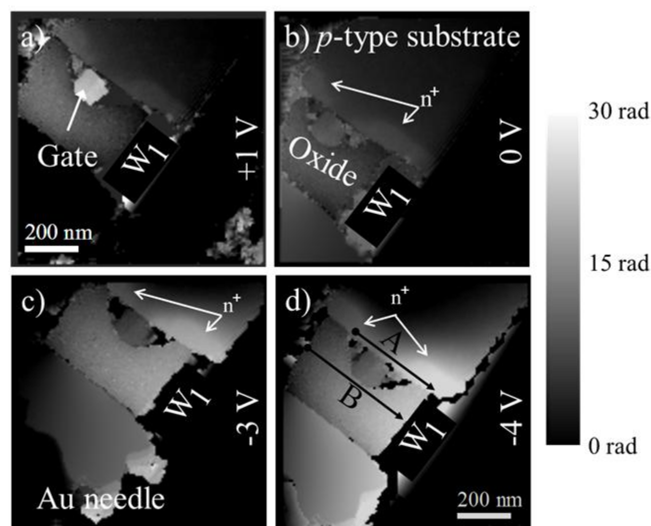

Figure 2) Phase images acquired from transistor T_1 (marked in Fig.1a) under different biasing conditions. The *pn* junction between the n^+ drain region under the W_1 plug at the corner of the specimen and the *p*-type substrate was electrically biased, from 1V forward bias in a) to 4V reverse bias in d).

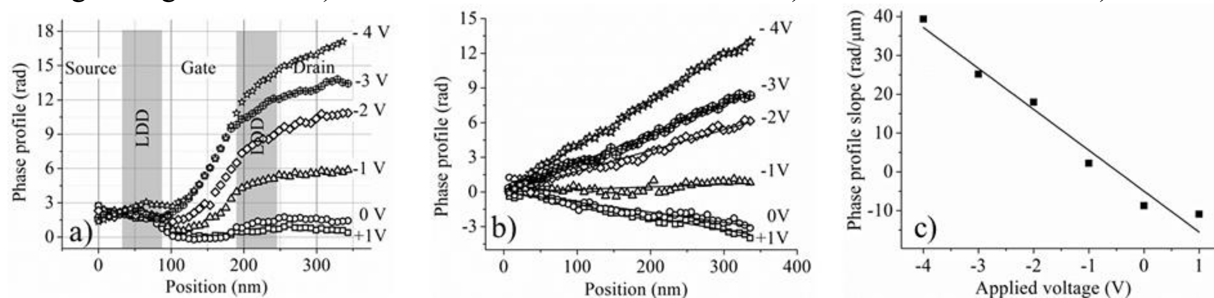

Figure 3) Phase profiles obtained from a) the source to the drain region under the gate (marked with the arrow A in Fig. 2d) and b) the oxide region above the gate (marked with the arrow B in Fig. 2d) as a function of biasing voltage. c) The slope of the lines fitted to the phase profiles in b) as a function of biasing voltage.

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