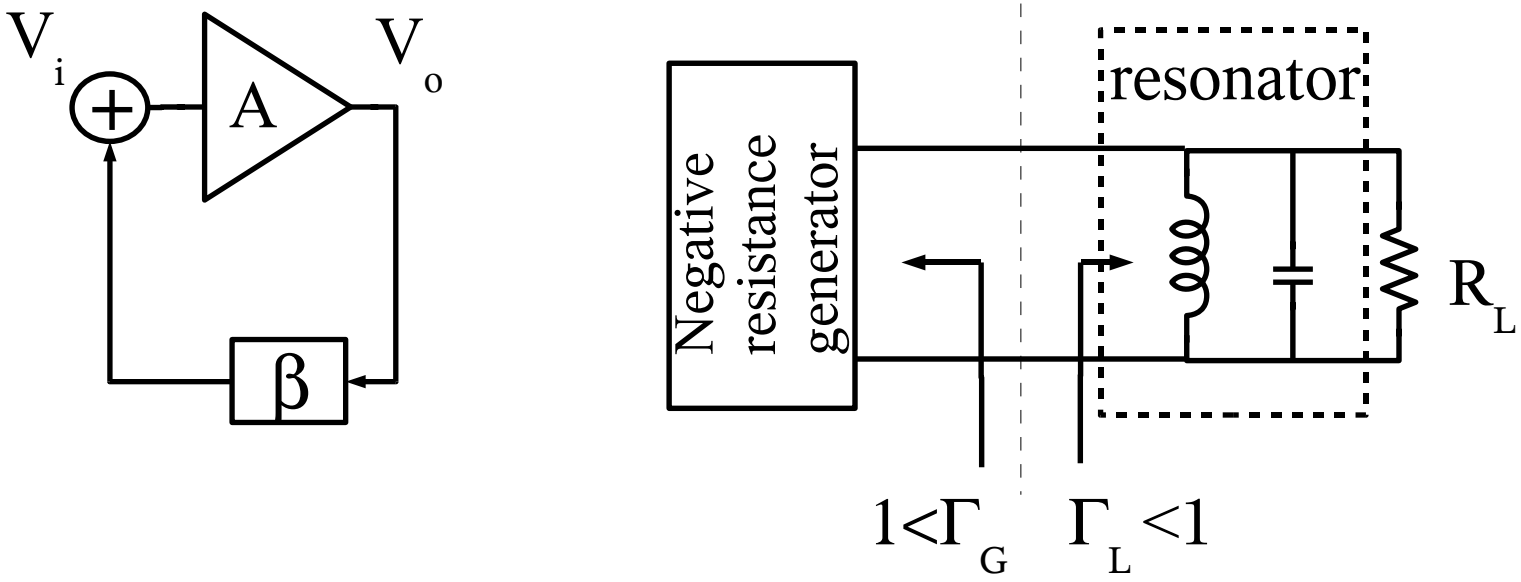
High Frequency VCO Design

Outline

- VCO fundamentals
- Low-noise LC VCO topologies
- VCO design methodology
- Examples of VCOs above 10 GHz
- CMOS VCO Design Scaling over Frequency

VCO Fundamentals: oscillator model



- Amplifier with selective (positive) feedback or
- Negative resistance single-port in parallel with resonant tank

Oscillation condition: linear feedback model

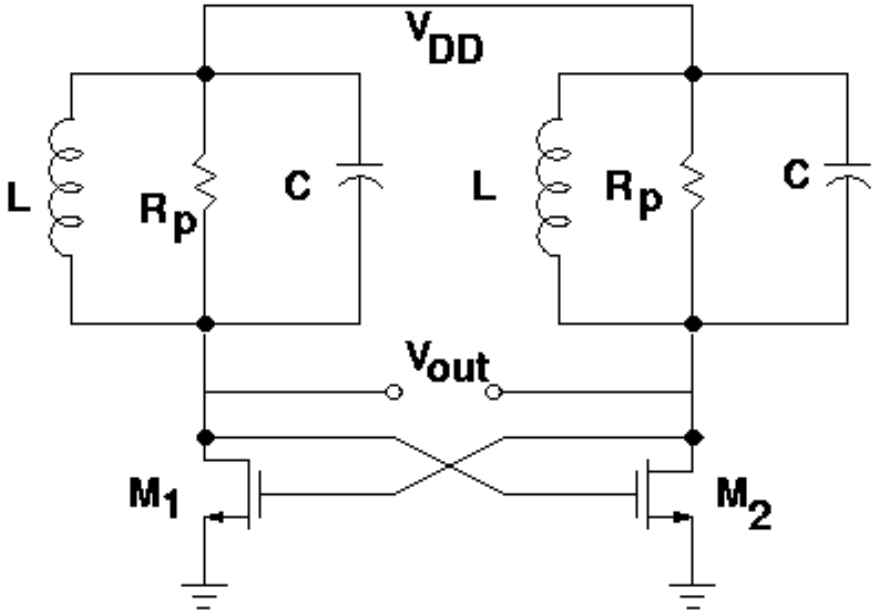
- Amplifier with (selective) feedback model Barkhausen's (or Nyquist's) criterion

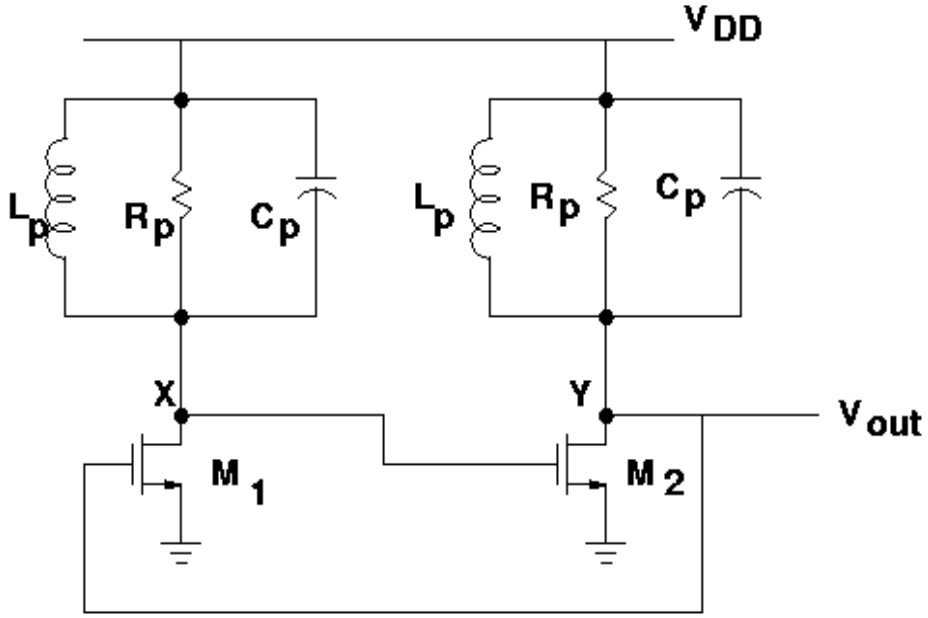
$$V_{osc} = \frac{A(V_{osc}, \omega)}{1 - \beta(V_{osc}, \omega) A(V_{osc}, \omega)} V_i$$

$$\left|\beta(\omega_{osc}) A(0)\right| > 1 ; \left|\beta(\omega_{osc}) A(V_{osc})\right| = 1 ; \quad \text{PHASE}[\beta(\omega_{osc}) A] = 360^{o}$$

- The amplitude of the oscillation is stabilized by the nonlinearity of the transistors in the amplifier

Example: Cross-coupled oscillator



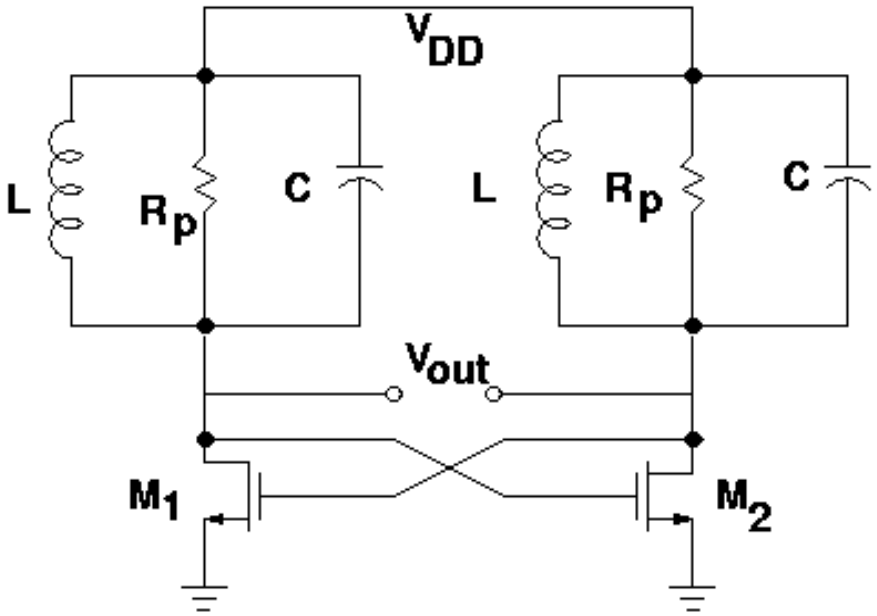


$$A(\omega_{osc})=(-g_m R_p)\times(-g_m R_p) \qquad \beta(\omega)=1 \qquad \omega_{osc}=\frac{1}{\sqrt{LC}} \qquad g_m R_P>1$$

$$1<g_m R_P=\frac{g_m}{g_o+\dfrac{1}{Q\omega_{osc}L}}=\frac{g'_m W}{g'_o W+\dfrac{1}{Q\omega_{osc}L}}=\frac{g'_m}{g'_o+\dfrac{1}{WQ\omega_{osc}L}}$$

$$W>\frac{1}{(g'_m-g'_o)Q\omega_{osc}L}$$

Example: 60 GHz in 65-nm CMOS



- J_{opt} = 0.15 mA/μm,
- g'_m = 1mS/μm; g_o=0.2mA/μm,
- L=50 pH, Q =10
- Note: In reality Q= 2-3 at 60 GHz

$$C = \frac{1}{L(2\pi f_{osc})^2} = \frac{1}{5\times10^{-11}(6.28\times6\times10^{10})^2} = 141fF$$

$$W > \frac{1}{(g'_m - g'_o)Q\omega_{osc}L} = \frac{1}{0.0008\times10\times6.28\times6\times10^{10}\times5\times10^{-11}} = 6.63\mu m$$

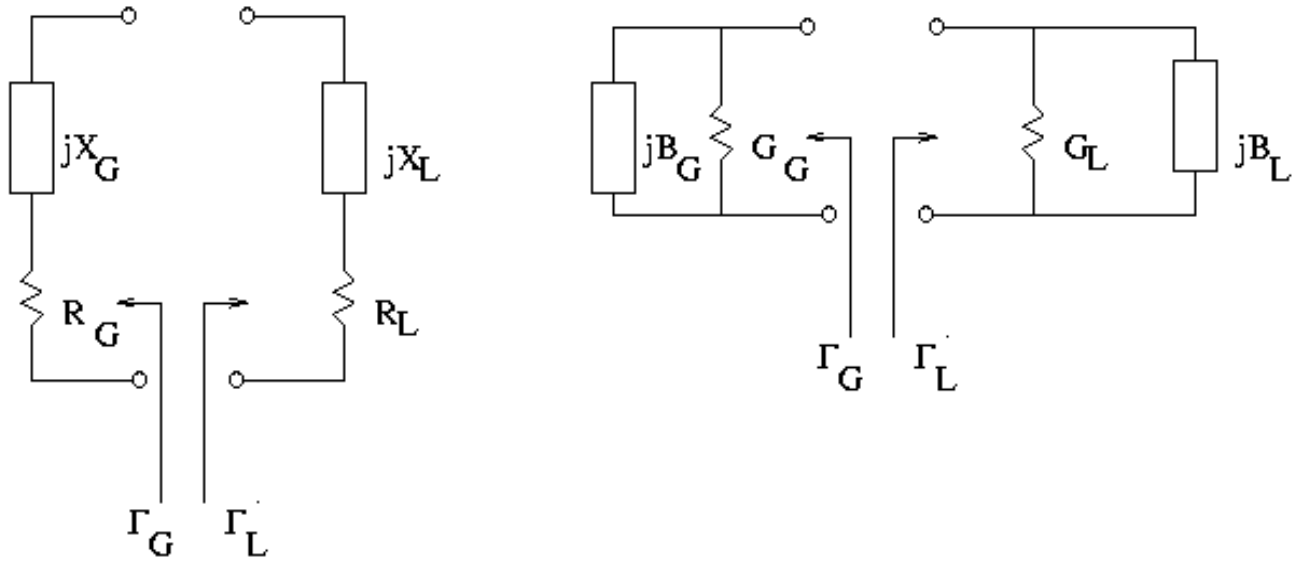
I_{DS} >= 1mA

Oscillation condition: negative resistance model

- Negative resistance single-port model

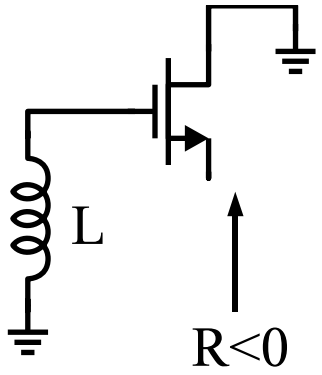
$$|R_G(0)|>3R_L(\omega_{osc});\quad R_G(V_{osc})+R_L(\omega_{osc})=0;\quad X_G(V_{osc},\omega_{osc})+X_L(\omega_{osc})=0$$

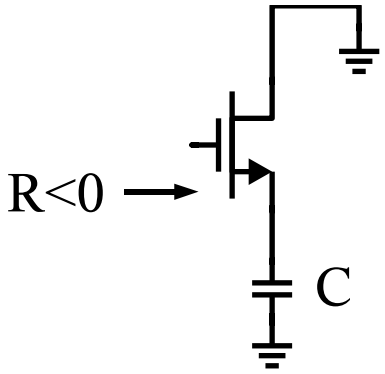
$$|G_G(0)|>3G_L(\omega_{osc});\quad G_G(V_{osc})+G_L(\omega_{osc})=0;\quad B_G(V_{osc},\omega_{osc})+B_L(\omega_{osc})=0$$

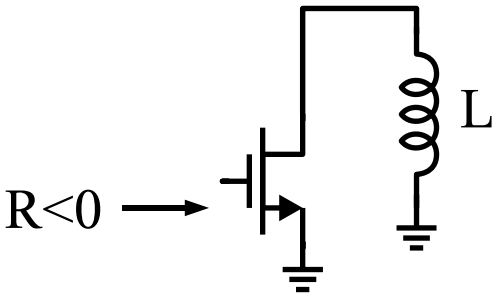


- The amplitude is stabilized by the nonlinearity of the negative resistance device

Methods to generate negative resistance







$$R \approx \frac{1}{g_m} - \frac{\omega^2 L_B}{\omega_T}$$

$$R \approx \frac{-\omega_T}{\omega^2 C}$$

$$R \approx \frac{1}{g_m} - \frac{\omega^2 L}{\omega_T (1 - \omega^2 C_{gd} L)}$$

$$L > \frac{1}{\omega^2 (C_{gd} + C_{gs})}$$

- Adding reactive elements at appropriate transistor terminals (three topologies above)
- Cross-coupled structure with positive feedback

Example: 60-GHz VCO in 65-nm CMOS

- Assume W=50μm, g_m= 50mS, C_{gs} =30fF, C_{gd}=15fF
- Calculate L min for Gate-GND inductance

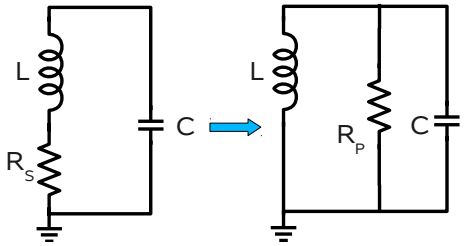
$$L > \frac{1}{(6.28\times 6\times 10^{10})^2 (15+30)\times 10^{-15}} = 156.51pH$$

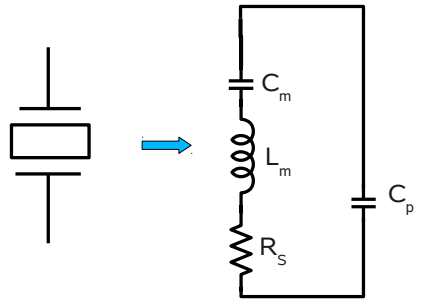
L =0.3nH => R=-50.77 Ohm (but R_s+R_g = 8 Ohm)

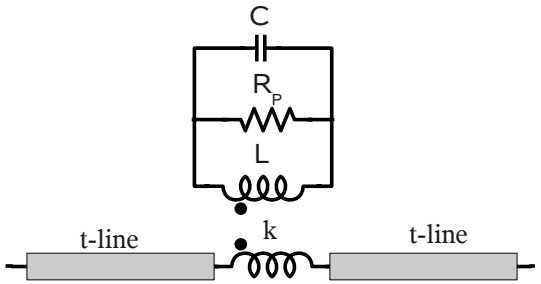
VCO Fundamentals: resonators

- High Q (>1000) but not yet integrated in ICs
  - Dielectric puck (high ε_R) -add varactor
    - ferroelectric materials “hot” for tunable resonators
  - Magnetic & widely (octave) tunable:
    - Ferrite YIG (yittrium-iron-garnet) sphere
    - MSW (magnetostatic wave) thin film
- Low Q (<100) affording integration in ICs
  - Lumped LC - tunable with varactor C
  - T-line with varactor loading for tunability

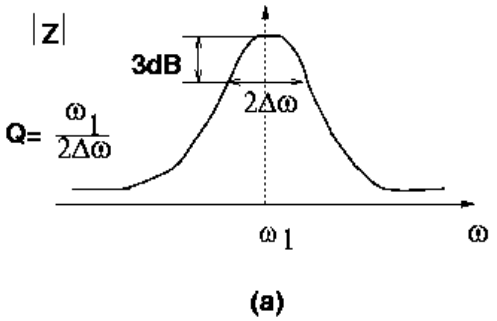
Resonator models





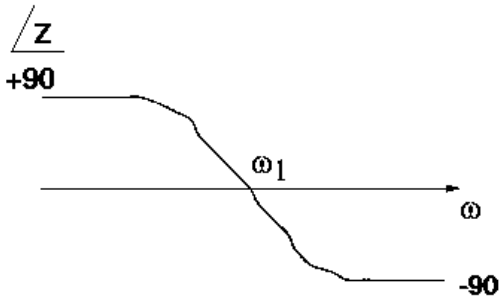


LC-tank Quartz crystal Dielectric resonator



(a)

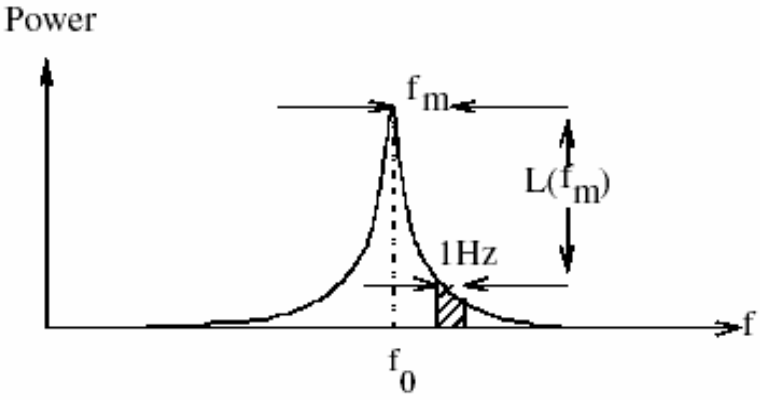
$$R_p \approx R_s Q^2$$



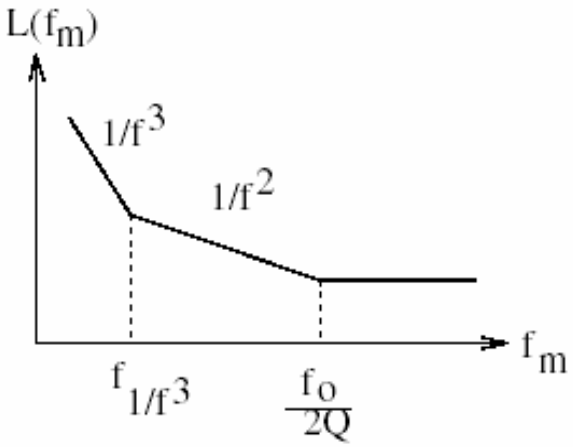
(b)

For inductor: $R_p = \omega_1 LQ$

VCO Fundamentals: phase noise definition



Output power spectrum of differential LC-Tuned VCO



Phase noise variation with frequency offset

- Phase noise is a measure of oscillator stability and refers to short-term random fluctuations in *f* or ϕ
- Phase noise is defined as the single-sideband power at a frequency offset f_m from the carrier frequency f_o measured in a 1Hz band compared to the carrier power

Phase noise as frequency modulation

- The output voltage of the oscillator can be expressed as:

$$v_o(t) = V_{osc}\cos[\omega_{osc}t + \theta(t)]$$

where $\theta(t)$ represents the random phase fluctuation

Small phase fluctuations can be represented as:

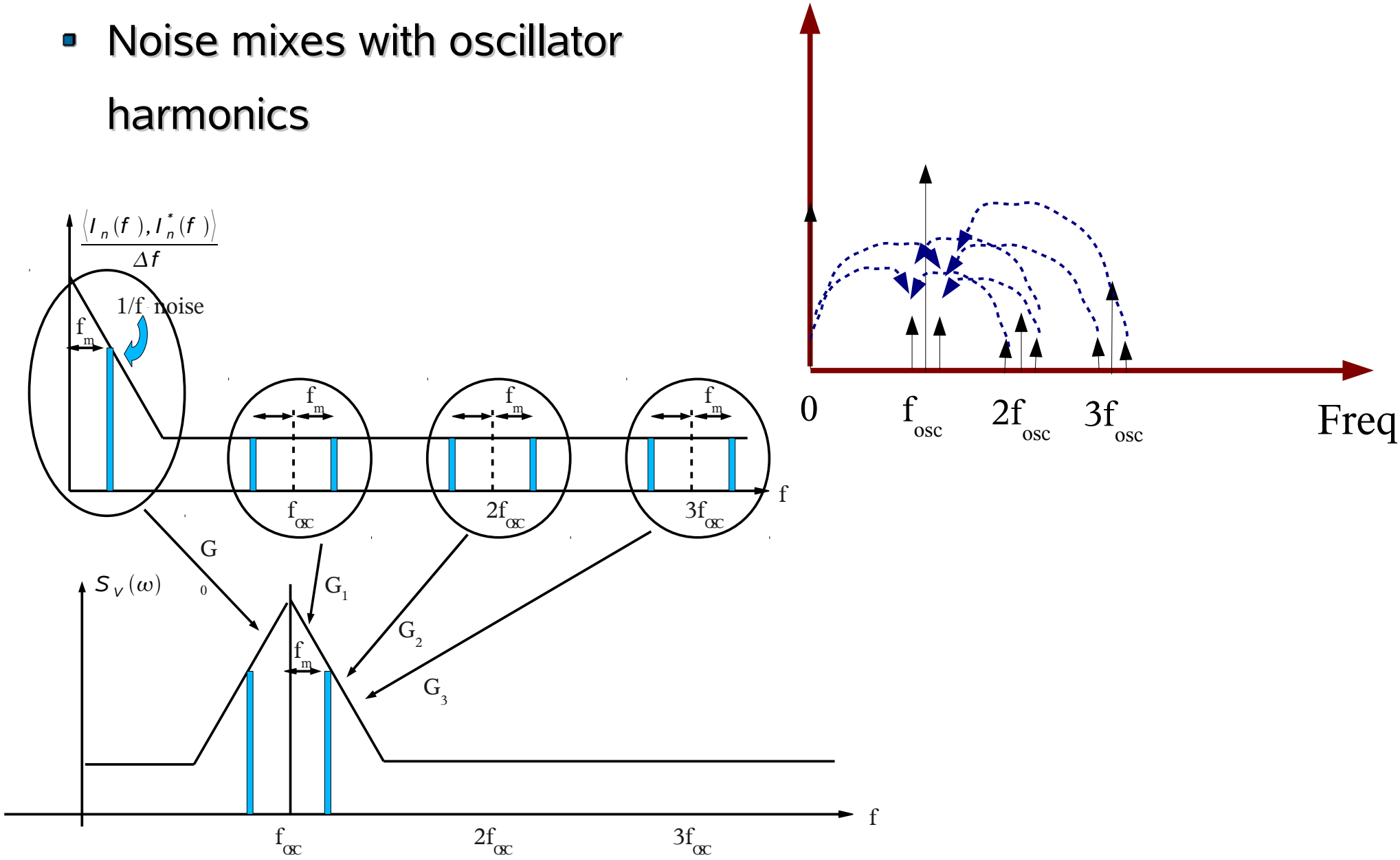
resulting in $$\theta(t) = \frac{\Delta f}{f_m}\sin\omega_m t = \theta_p \sin\omega_m t$$

$$v_o(t) = V_{osc}\left\{\cos(\omega_{osc}t)\cos[\theta_p \sin(\omega_{osc}t)] - \sin(\omega_{osc}t)\sin[\theta_p \sin(\omega_{osc}t)]\right\}$$

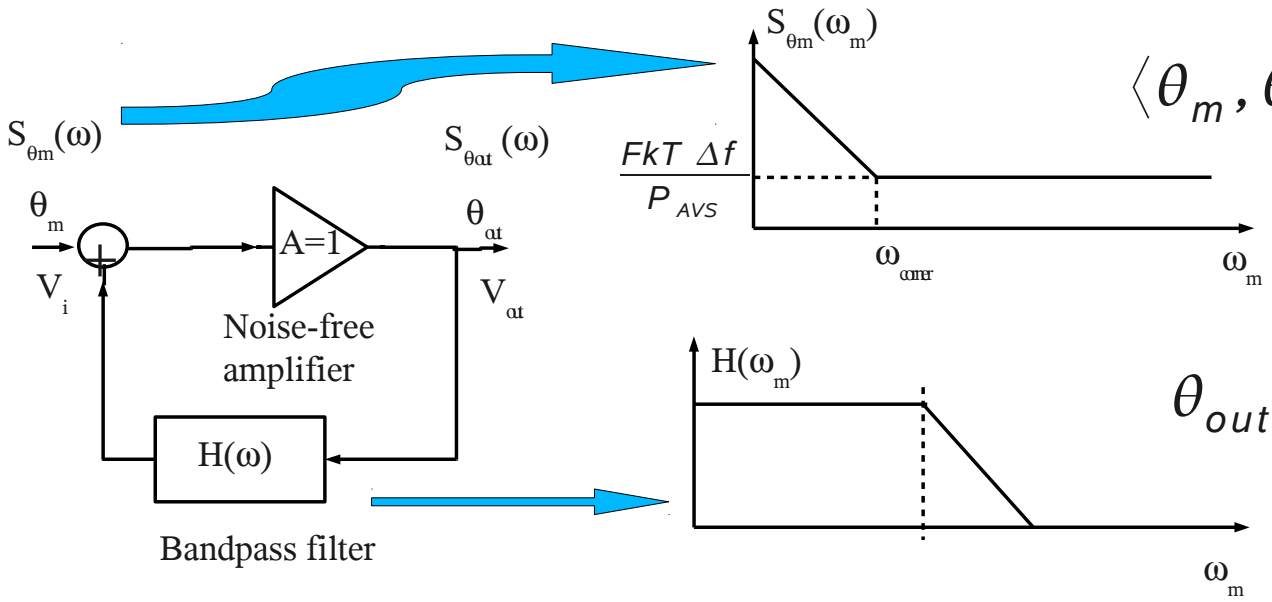
$$v_o(t) \approx V_{osc}\left\{\cos(\omega_{osc}t) - \frac{\theta_p}{2}\left\{\cos[(\omega_{osc}+\omega_m)t] - \cos[(\omega_{osc}-\omega_m)t]\right\}\right\}$$

Phase noise as noise mixing

- Noise mixes with oscillator harmonics



VCO Fundamentals: Leeson's phase noise model (Pozar Ch. 12.3, pp.594-599)



$$\langle \theta_m, \theta_m \rangle = FkT\,\Delta f\left(1+\frac{f_{corner}}{f_m}\right)$$

$$f_m = f - f_{OSC}$$

$$\theta_{out}(f_m)\times H(f_m)+\theta_m=\theta_{out}(f_m)$$

$$H(jf)=\frac{1}{1+jQ\left(\frac{f}{f_{OSC}}-\frac{f_{OSC}}{f}\right)} \quad \text{hence } H(jf_m)\approx\frac{1}{1+j\frac{2f_mQ_L}{f_{OSC}}}$$

$$\theta_{out}(f_m)=\frac{\theta_m}{1-H(f_m)}=\theta_m\frac{1+j\frac{2f_mQ_L}{f_{OSC}}}{j\frac{2f_mQ_L}{f_{OSC}}}=\theta_m\left(1-j\frac{f_{OSC}}{2f_mQ_L}\right)$$

Leeson's phase noise formula

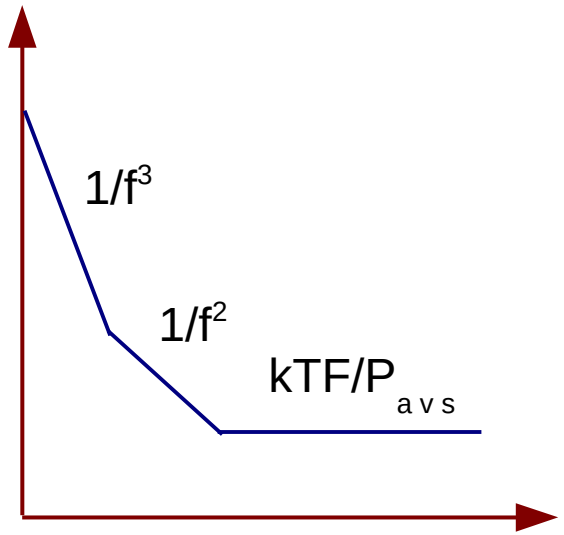
$$P_{noise} = \langle \theta_{out}, \theta_{out} \rangle = \langle \theta_m, \theta_m \rangle \left[1 + \left(\frac{f_{OSC}}{2 f_m Q_L} \right)^2 \right]$$

$$\mathcal{L}(f_m) = \frac{P_{noise}}{P_{AVS}} = \frac{\frac{1}{2}\left(\frac{V_{osc}\theta_p}{2}\right)^2}{\frac{1}{2}V_{osc}^2} = \frac{\theta_p^2}{4} = \frac{\theta_{rms}^2}{2} = \frac{FkT\Delta f}{2P_{avs}}\left[1 + \left(\frac{f_{osc}}{2Q_L f_m}\right)^2\right]\left(1 + \frac{f_{corner}}{f_m}\right)$$

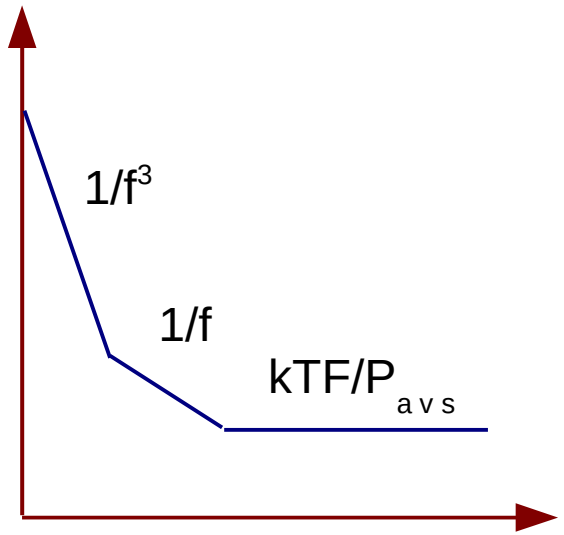
- Q_L = resonator loaded Q; P_{avs} = average signal power
- P_{noise} = noise power in a single sideband of 1 Hz
- f_m = frequency offset from f_{osc}
- F = transistor (amplifier) noise factor with respect to resonator impedance @ resonance
- f_{corner} = flicker noise corner frequency
- Δf = noise measurement bandwidth = 1 Hz

Leeson's phase noise formula

- Indicates that there can be 4 regions in the L(f) characteristics:
  - 1/f
  - $1/f^2$
  - $1/f^3$
  - f^0



Low Q



high Q

Phase noise contributors

- Resonator *Q*. Higher is better.
- Oscillation amplitude. Higher is better.
- Transistor noise. Lower is better.
- Amplitude limitation mechanism (linearity). Avoid HBT saturation.
- Bias supply, current tail & tuning control noise. (differential control and topology is better).
- Buffer amplifier (load) noise. Loading the tank directly is bad for noise.

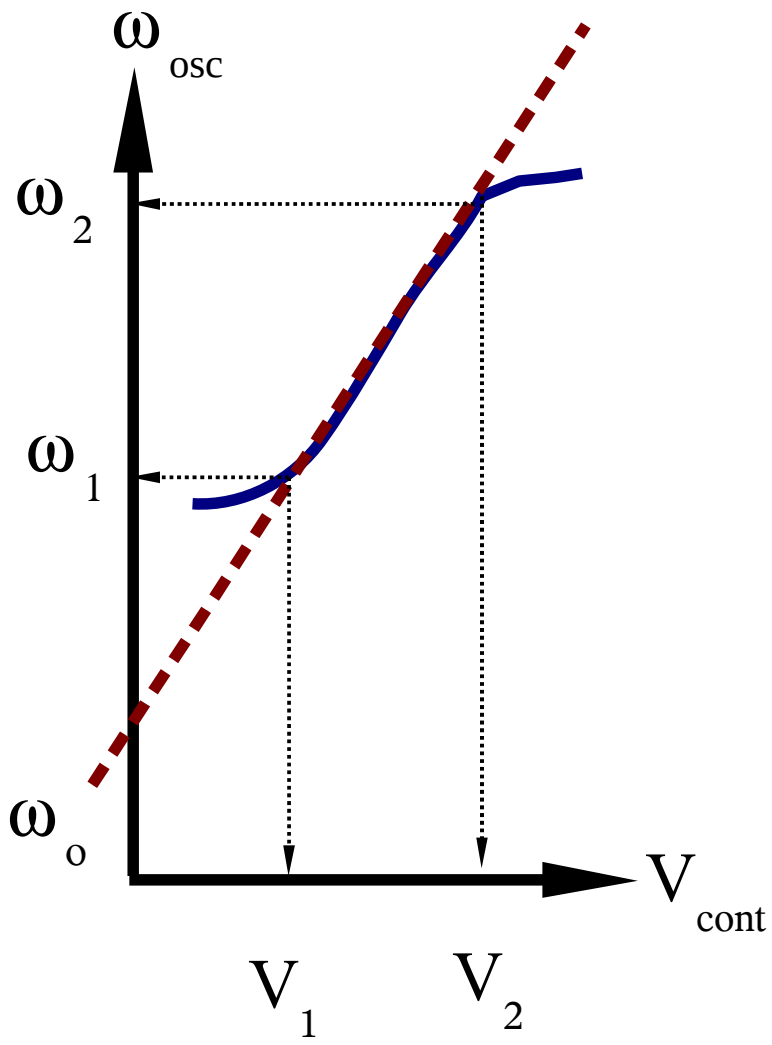
VCO Fundamentals: frequency tuning

- Want tunable oscillators:

$$\omega_{osc} = \omega_0 + K_{VCO} V_{cont}$$

- $\omega_2 - \omega_1$ = tuning range
- $V_2 - V_1$ = control range
- K_{VCO} = VCO gain (sensitivity)

$$K_{VCO} > \frac{\omega_2 - \omega_1}{V_2 - V_1}$$



VCO Fundamentals: specification

- Center frequency: f_{osc}
- Tuning range: $(f_2 - f_1)/f_{osc}$
  - large to cover process variation
  - small to reduce phase noise
  - K_{VCO} increases with center frequency and lower supply voltage. So does phase noise.
  - Want constant K_{VCO} over tuning range in PLL design
- Tuning linearity (important for PLLs)
  - Can use linearization techniques

RF VCO Fundamentals: specification

- Phase noise (dBc/Hz)
  - translates in jitter
  - easier to measure than jitter
- Output amplitude/power
  - larger is better to reduce noise
  - trade-off with supply voltage and power
  - May vary across tuning range (bad)
- Power dissipation

RF VCO Fundamentals: specification

- **Supply rejection**: **pushing**

$$\frac{\Delta \omega_{osc}}{\Delta V_{supply}}$$

  - lower is better
  - differential topology helps
  - Common mode rejection helps
- **Load mismatch rejection**: **pulling**

$$\frac{\Delta \omega_{osc}}{\Delta \Gamma_{L}}$$

  - lower is better
  - Improved by better transistor isolation and/or buffer amplifier between VCO and load
- **VCO figures of merit**

$$FoM_1 = \left(\frac{f_{osc}}{f_m}\right)^2 \frac{1}{L(\Delta f) P_{DC}}$$

$$FoM_2 = \left(\frac{f_{osc}}{f_m}\right)^2 \frac{P_{AVS}}{L(\Delta f) P_{DC}}$$

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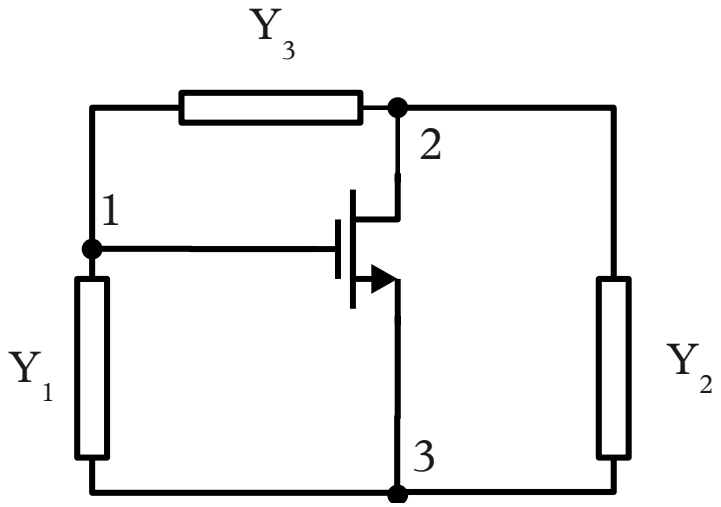
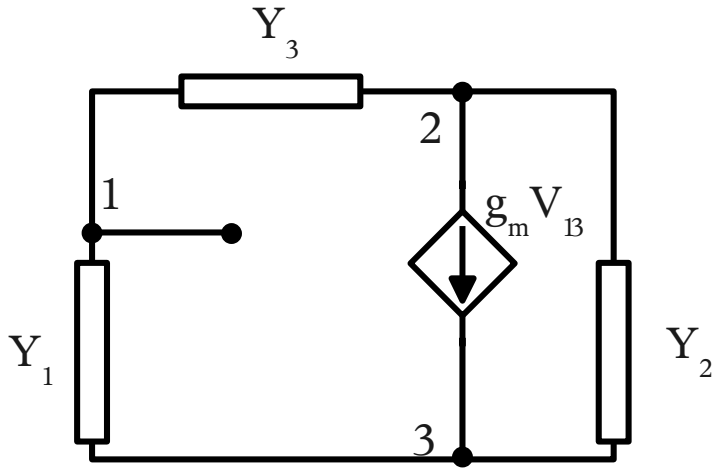
LC VCO topologies

- Selective feedback (L, C, Transformer):
  - Colpitts (2C + 1L)
  - Clapp (2C+1LC)
  - Armstrong (1C + xfmr)
  - Hartley (1C + 2L)
- Negative g_m or cross-coupled with tuned amplifier and unity feedback.

LC VCO topologies: Selective feedback





$$\begin{bmatrix} Y_1+Y_3 & -Y_3 & -Y_1 \\ G_m-Y_3 & Y_2+Y_3 & -G_m-Y_2 \\ -G_m-Y_1 & -Y_2 & G_m+Y_1+Y_2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$$

V_1, V_2, or V_3=0

$$\begin{bmatrix} G_m-Y_3 & -G_m-Y_2 \\ -G_m-Y_1 & G_m+Y_1+Y_2 \end{bmatrix} = 0$$

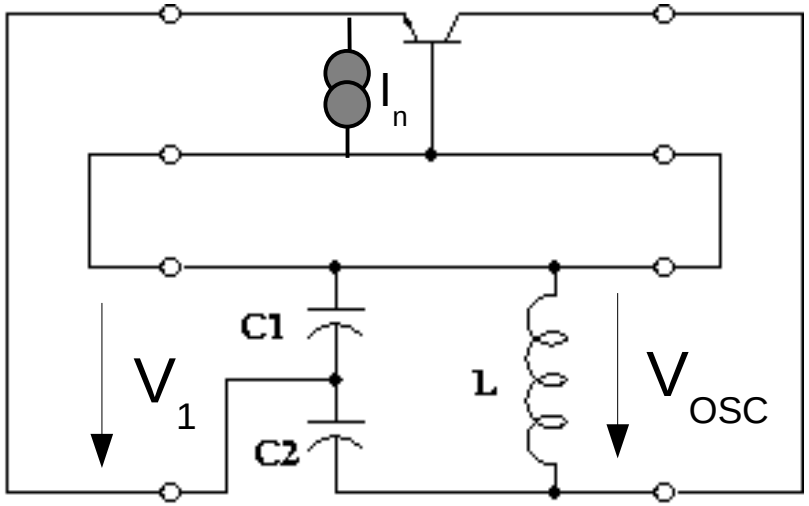
$$G_m Y_3 + Y_1 Y_2 + Y_1 Y_3 + Y_2 Y_3 = 0$$

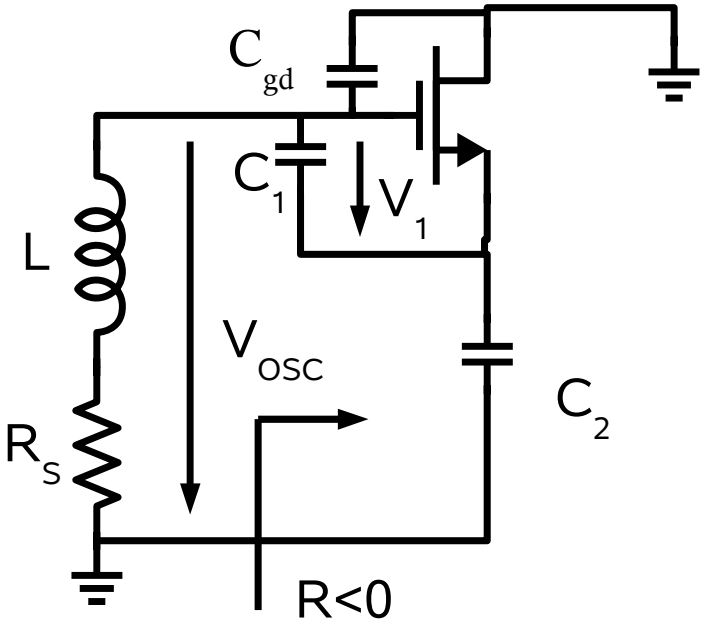
$$\frac{G_m}{G_0} = -\left(1+\frac{B_1}{B_3}\right) = \frac{B_1}{B_2}$$

$$\frac{1}{B_1}+\frac{1}{B_2}+\frac{1}{B_3}=0$$

Colpitts topology

- Use feedback or negative resistance model
- R_s is the loss resistance of the inductor





$$R = \frac{-g_m}{\omega^2 C_1 C_2}$$

$$R_S = \frac{\omega_{osc} L}{Q}$$

Colpitts topology

- Analysis at oscillation condition is carried out using large signal equivalent model for transistor
- G_m is the large signal transconductance
- V_1 is the amplitude of the voltage across C_1
- I_{BIAS} is the transistor bias current

$$G_m \approx \frac{2I_{BIAS}}{V_1}$$

$$\frac{G_m}{\omega_{osc}^2 C_1 C_2} = R_S \text{ or } G_m R_P = \frac{(C_1 + C_2)^2}{C_1 C_2} \geq 4$$

$$\frac{1}{f_{osc}} = 2\pi\sqrt{L\left[C_{gd} + \frac{C_1 C_2}{C_1 + C_2}\right]} \approx 2\pi\sqrt{\frac{L C_1 C_2}{C_1 + C_2}}$$

$C_1 \gg C_\pi (C_{gs})$ to avoid pushing

$$L(f_m) = \frac{|I_n|^2}{V_{osc}^2} \times \frac{1}{f_m^2} \times \frac{1}{C_1^2\left(\frac{C_1}{C_2} + 1\right)^2}$$

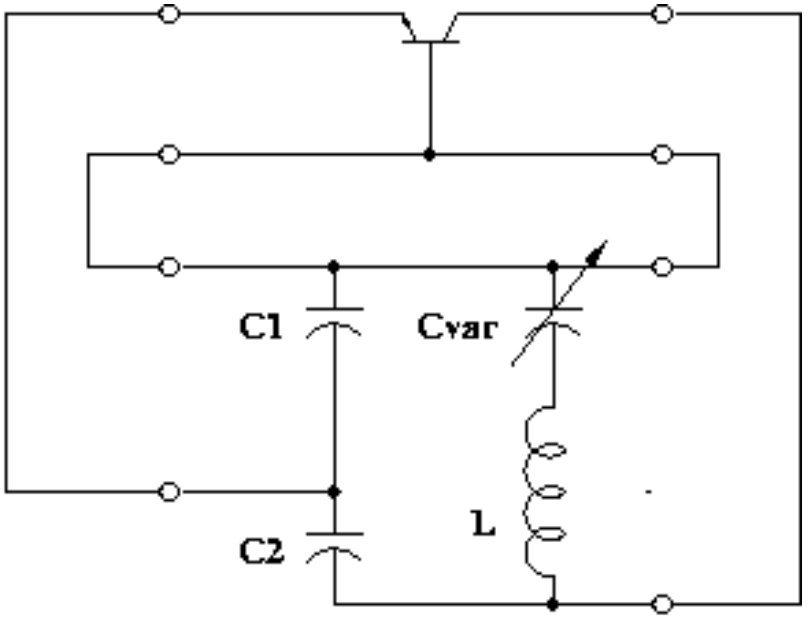
LC VCO topologies: Selective feedback

- To reduce noise, V_1 and V_2 should be as large as possible (limited by transistor breakdown)
- V_{osc} can be larger than the supply voltage but not larger than the transistor breakdown voltage
- V_1 depends on inductor (tank) Q and bias current

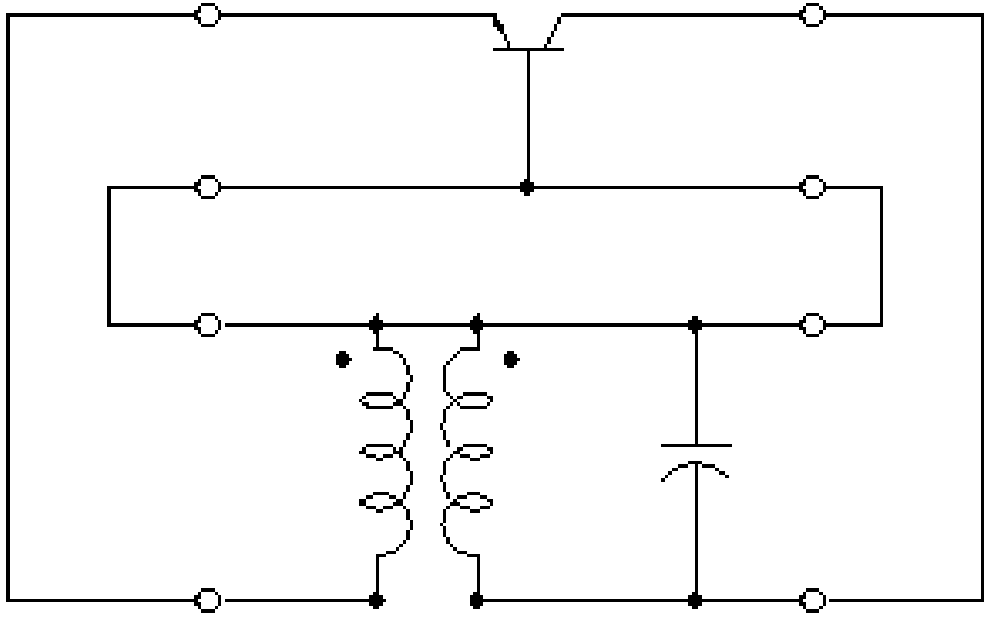
$$\frac{G_m}{\omega_{osc}(C_1+C_2)}=\frac{1}{Q} \qquad V_1 \approx \frac{2I_{BIAS}Q}{\omega_{osc}(C_1+C_2)} \qquad V_{osc}=V_1\left(1+\frac{C_1}{C_2}\right)=\frac{2I_{BIAS}Q}{C_2\omega_{osc}}$$

$$L(f_m)=\frac{|I_n|^2}{V_{osc}^2}\times\frac{1}{f_m^2}\times\frac{1}{C_1{}^2\left(\frac{C_1}{C_2}+1\right)^2}=\frac{|I_n|^2\omega_{osc}^2}{I_{BIAS}^2 f_m^2 4Q^2}\frac{C_2{}^2}{C_1{}^2}\times\frac{1}{\left(\frac{C_1}{C_2}+1\right)^2}$$

Other selective feedback topologies

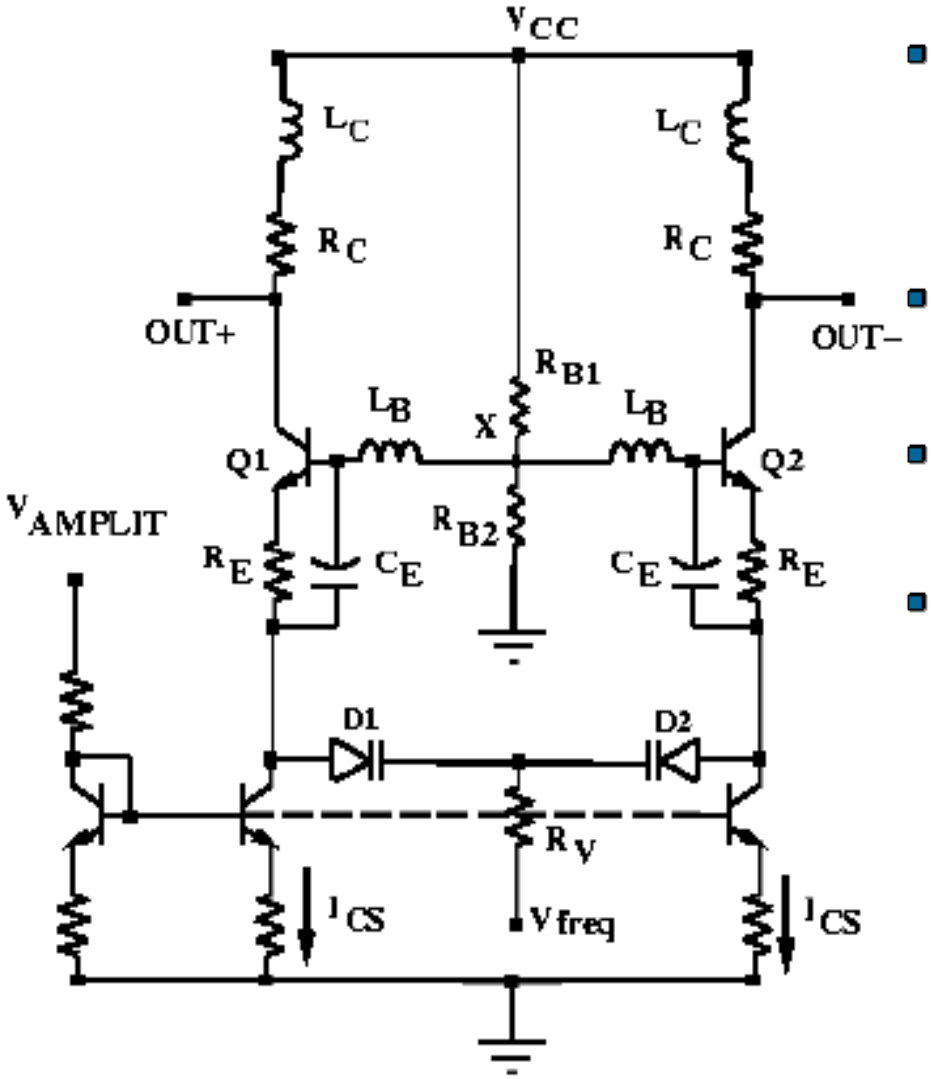


Clapp



Armstrong

SiGe HBT: differential Colpitts topology



- Negative resistance transistors $Q_{1,2}$ also act as buffer -> low noise.
- HBT sized and biased for optimal noise
- Emitter degeneration R_E for linearity
- Operation on 2nd. harmonic of the LC-varactor tank is possible (push-push)

L. Dauphinee, M.Copeland, ISCC 1997.

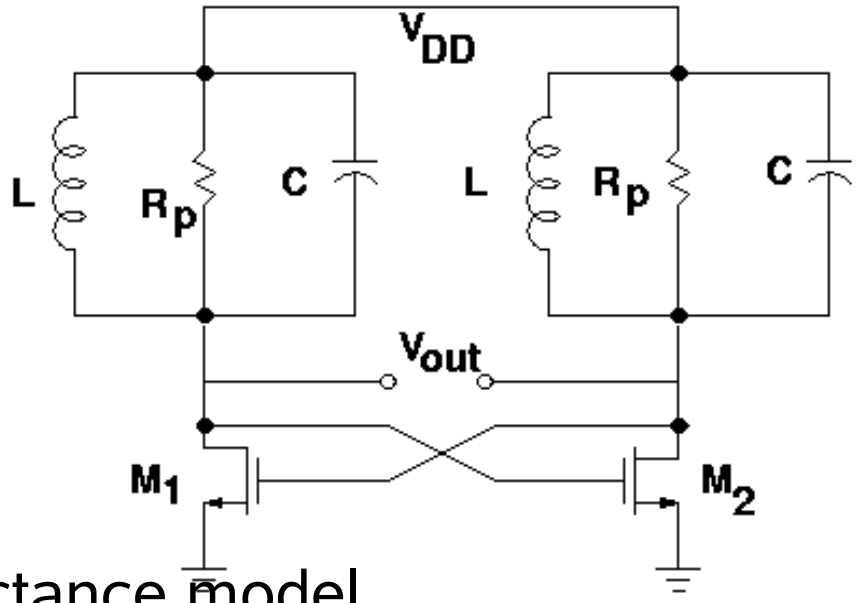
LC VCO topologies: Cross-coupled

- Works well with both MOSFETs and HBTs
- Favoured in MOSFET implementations

$$G_m \approx \frac{4 I_{BIAS}(M1)}{V_{out}}$$

- Oscillation condition: $(g_m R_P)^2 > 1$

$$Y_{out} = \frac{-G_m}{2} + j\omega\left(\frac{C_{gs}}{2} + \frac{C_{db}}{2} + 2C_{gd}\right)$$



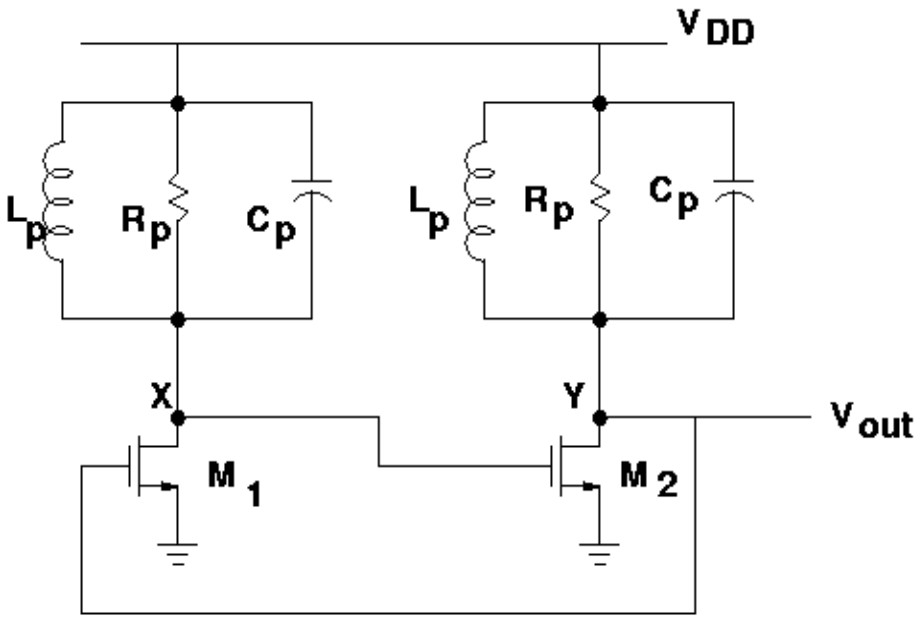
- Oscillation frequency:

$$f_{osc} = \frac{1}{2\pi\sqrt{L(C + C_{gs} + C_{db} + 4C_{gd})}}$$

- Use feedback or negative conductance model

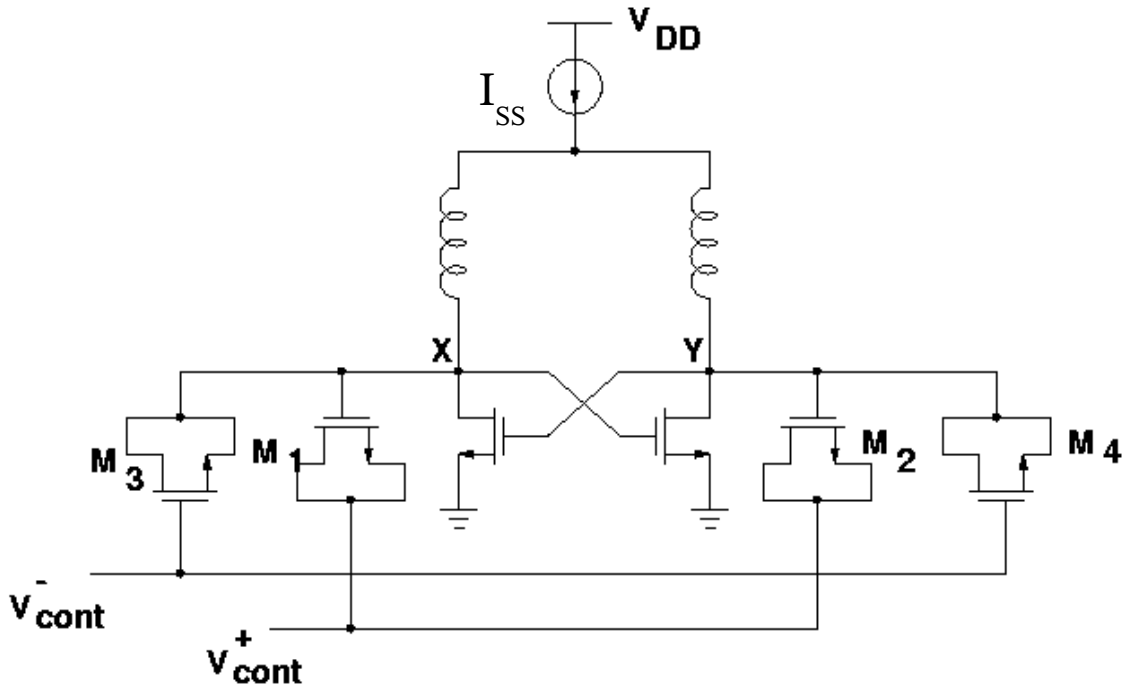
Cross-coupled VCO topology (cont.)

- Two stage selective amp. with positive feedback. Gain per stage at ω_{osc} is $-g_m R_p$
- Needs lower g_m than Colpitts to oscillate. Negative g_m increases with current.



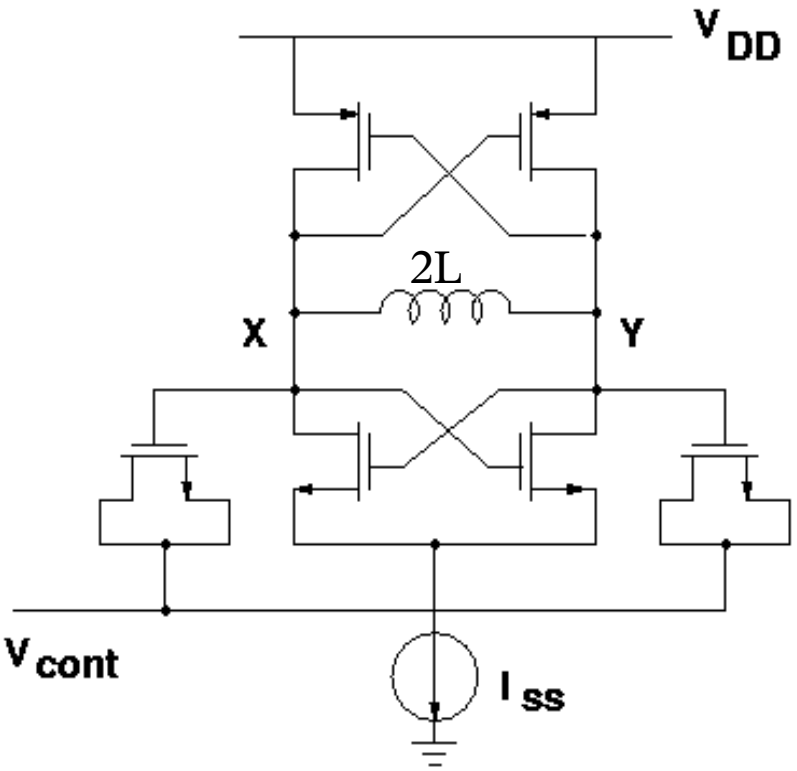
- Transistors sized & biased at minimum noise current density and optimal noise match to tank impedance. In HBT case must use de-coupling caps for separately biasing the bases of M1 and M2

MOS cross-coupled VCO topology (cont.)



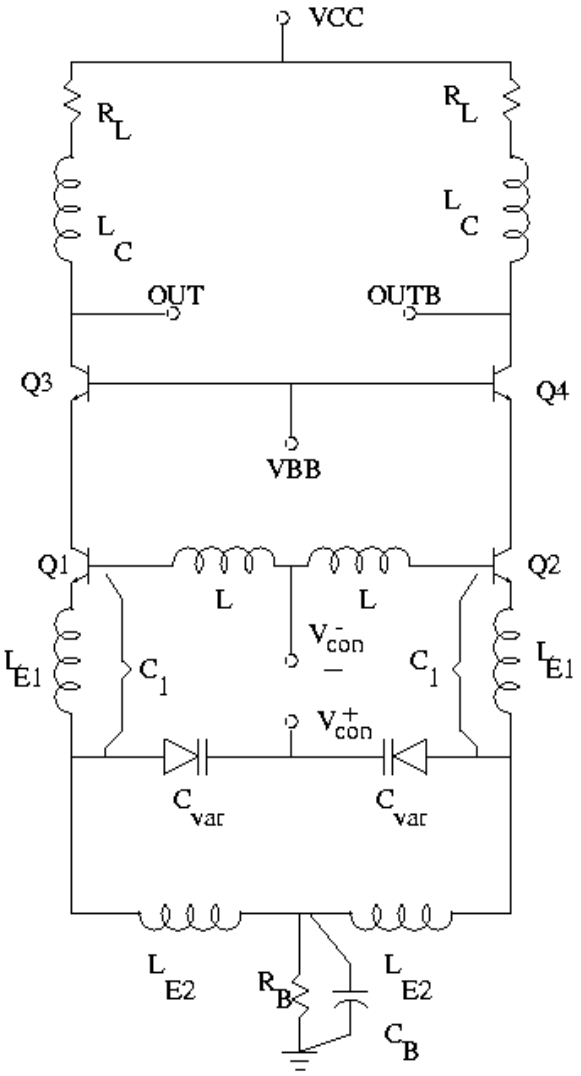
- $V_{osc}=I_{SS}R_{p,}$ No built-in load buffering. Buffer amplifier loads tank.
- Differential tuning control to reduce noise.
- Highest frequency: 300 GHz in 65-nm CMOS [B. Razavi JSSC 2011].

Cross-coupled VCO topology: symmetrical



- p-MOSFET and n-MOSFET cross-coupled pair to balance the output signal shape and reduce 1/f noise which is severe in MOSFET implementations
- Swing is (almost) rail to rail.
- Maximum frequency limited by p-MOSFET performance.
- Poor power supply rejection unless current source is introduced.

SiGe HBT Colpitts topology improvements
(C. Lee et al. CSICS-2004)



Add inductive peaking to improve gain at HF.

Replace current source tails with resistor R_B and capacitor C_B to reduce noise at DC and $2f_{osc}$ (Winkler, ISSCC-2003, and RFIC 2003)

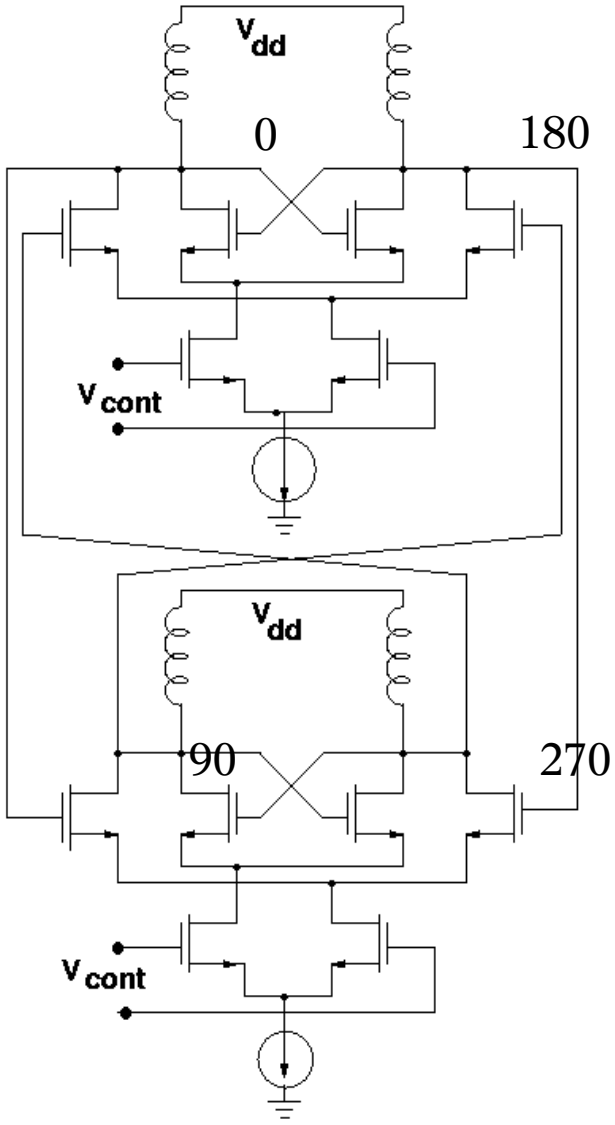
Replace resistive R_E with inductive emitter degeneration and add L_{E2} to reduce noise at f_{osc} and $2f_{osc}$ respectively (Li et al. JSSC Feb. 2003)

$$\frac{1}{2\pi\sqrt{L_{E1}C_{var}}} > f_{osc} \quad \text{and} \quad \frac{1}{2\pi\sqrt{L_{E2}C_{var}}} < f_{osc}$$

Add common base output buffer to improve isolation to load (Li et al. JSSC Feb. 2003)

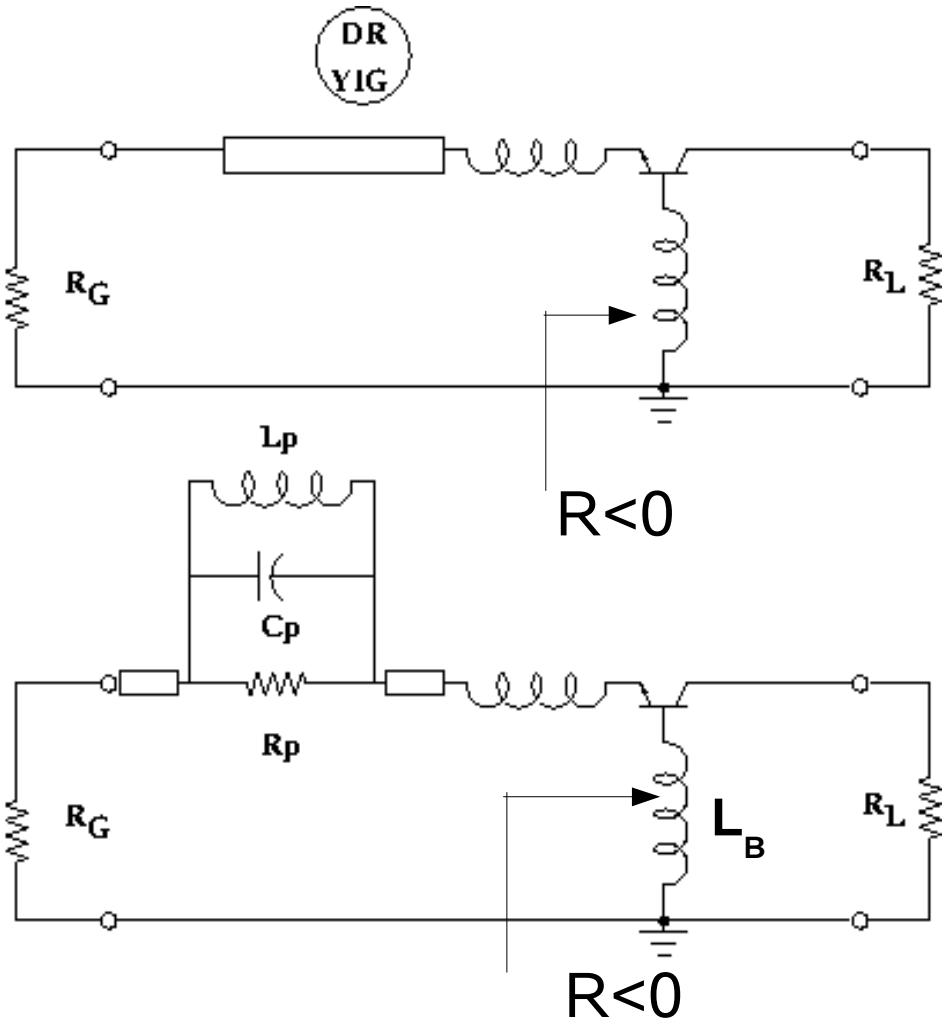
Apply control voltage differentially.

Quadrature VCOs: Cross-coupled



- Two, weakly-coupled VCOs.
- Output signals are 90° out of phase (in theory): inv. with inductive load
- Both tanks operate slightly off resonance hence noisier than single tank VCOs
- Frequency control implemented in current tails such that amplitude does not change with oscillation frequency
- Coupling must be at least 25%
- 8-phase topologies possible (see J.Lee & Razavi ISSCC 2003)

High Q resonator VCO topologies (hybrid ICs)



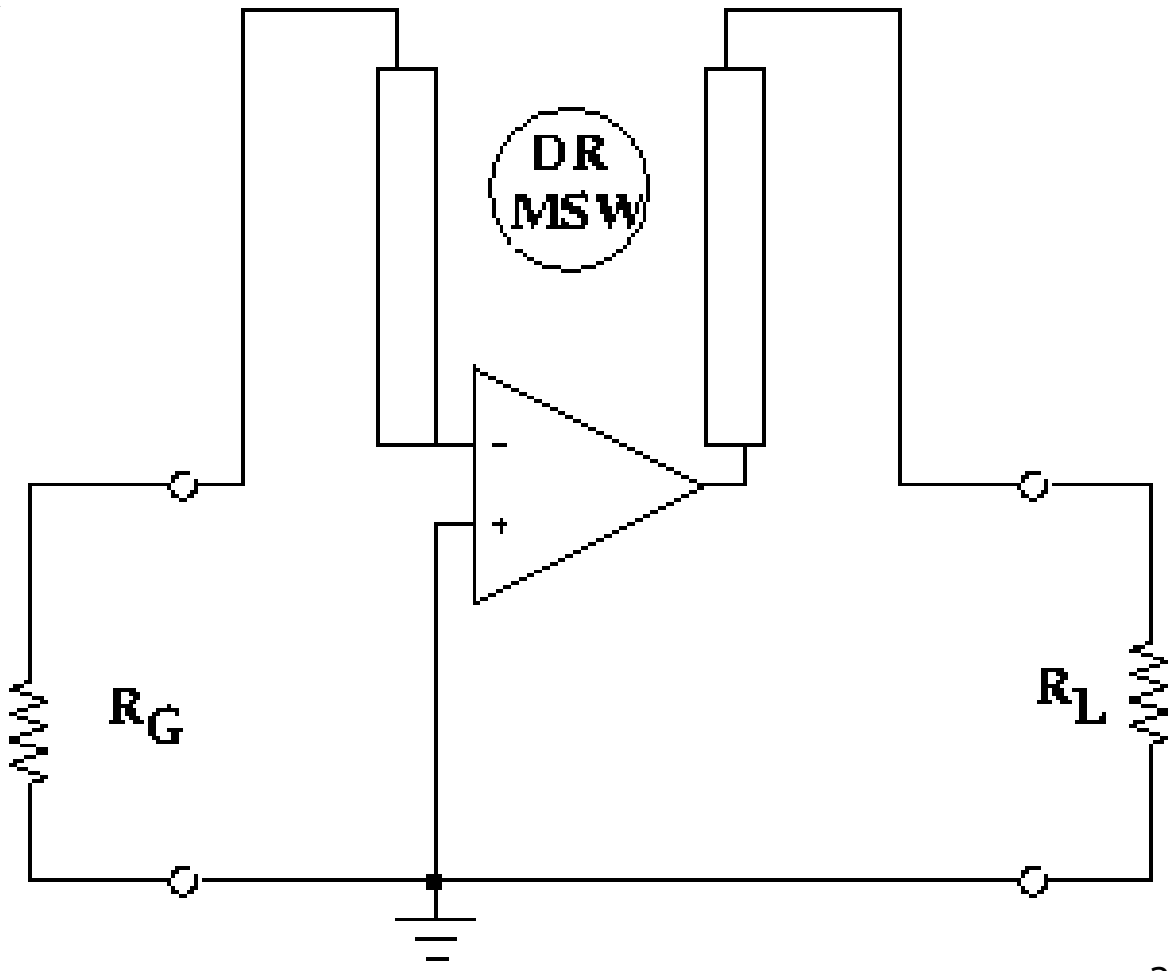
- Reflection line
  - negative resistance (common base/gate) transistor
  - resonator magnetically coupled to emitter/source t-line
  - Negative resistance model is preferred in analysis

$$R \approx \frac{1}{g_m} - \frac{\omega^2 L_B}{\omega_T}$$

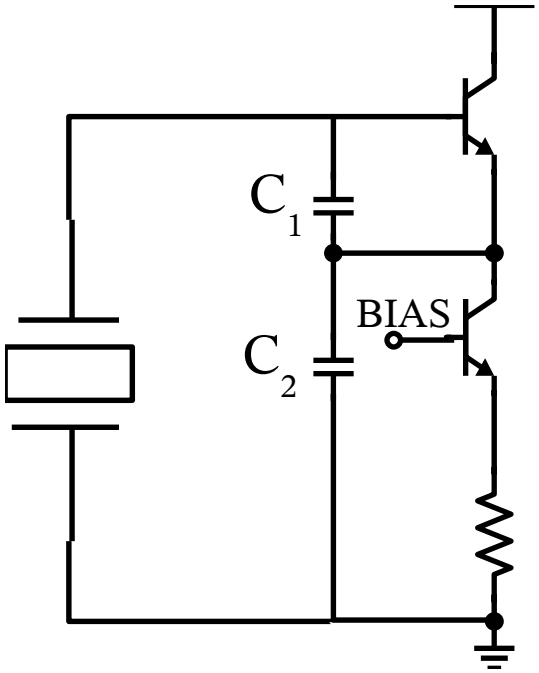
High Q resonator VCO topologies (hybrid ICs)

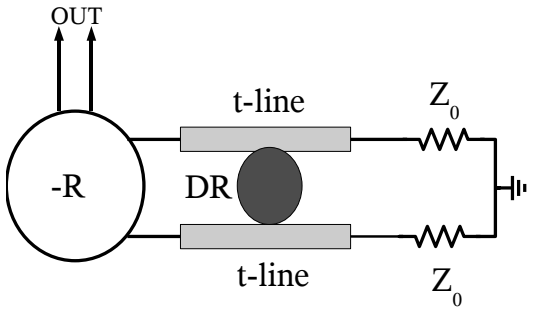
- Feedback
  - DR= dielectric resonator
  - MSW=magnetostatic wave

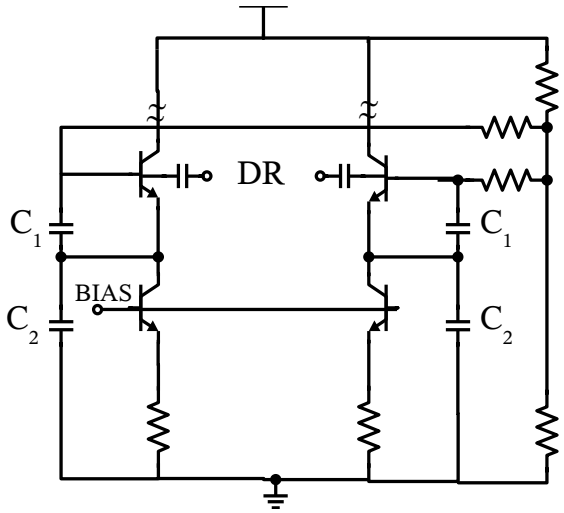
resonator



Clapp, crystal, DR oscillator topology







Infineon, IEEE BCTM 2008

Outline

- VCO fundamentals
- Low-noise LC VCO topologies
- **VCO design methodology**
- Examples of VCOs above 10 GHz.
- CMOS VCO design scaling over frequency

Colpitts VCO design methodology (as LNA)

Design philosophy

- Maximize oscillation amplitude V_{osc} on tank at resonance because it will minimize phase noise.

  i.e. set V_{osc} as the largest possible voltage allowed by the technology/power supply

- **Tradeoff:**
  - Low-power (maximum L, lowest bias current) or
  - Low-phase noise (lowest L, high bias current)

$$L(f_m) = \frac{|I_n|^2}{V_{osc}^2} \times \frac{1}{f_m^2} \times \frac{1}{C_1^2 \left(\frac{C_1}{C_2}+1\right)^2}$$

$$L(f_m) = \frac{|I_n|^2 \omega_{osc}^2}{I_{BIAS}^2 4Q^2} \frac{C_2^2}{C_1^2} \times \frac{1}{\left(\frac{C_1}{C_2}+1\right)^2}$$

Nallatamby et al., IEEE-trans. MTT, 2003
where I_n is the total noise current of transistor

VCO design methodology: Low power

P_{DC} is known, hence, in addition to V_{OSC}, I_{BIAS} is set.

(1)Bias transistor at J_{OPT} to minimize phase noise:

$W = I_{BIAS}/J_{OPT}$; $A_E = I_{BIAS}/J_{OPT}$

(2)R_{PMIN} L_{MIN} can now be calculated (cross-coupled)

$$R_{PMIN} = \frac{V_{OSC}}{2I_{BIAS}} \qquad L_{MIN} = \frac{R_{PMIN}}{Q\omega_{OSC}} = \frac{V_{OSC}}{2I_{BIAS}Q\omega_{OSC}}$$

(3) Calculate C_{eq} $$C_{eq} = \frac{1}{\omega_{OSC}^2 L}$$

VCO design methodology: Low phase noise

(1) Select L as small as possible.

(2) Once L is selected, C_{eq} is known and assuming Q determined by the back-end, R_p is also known.

(3) Since R_P and V_{OSC} are known, the minimum value of G_m can be estimated

$$\frac{G_m}{\omega_{osc}^2 C_1 C_2} = \frac{R_P}{Q^2} \Rightarrow \quad G_m R_P = \frac{(C_1 + C_2)^2}{C_1 C_2} \geq 4$$

and an initial guess on I_{BIAS} can be made assuming $C_1 = C_2 = 2C_{eq}$

$$G_m \approx \frac{2I_{BIAS}}{V_1} = \frac{2I_{BIAS}\left(1 + \frac{C_1}{C_2}\right)}{V_{OSC}} = 2\frac{I_{BIAS}}{V_{OSC}} C_1 L \omega_{osc}^2$$

(4) Bias at J_{OPT} for minimum phase noise => W, A_E

VCO design methodology: Low phase noise (ii)

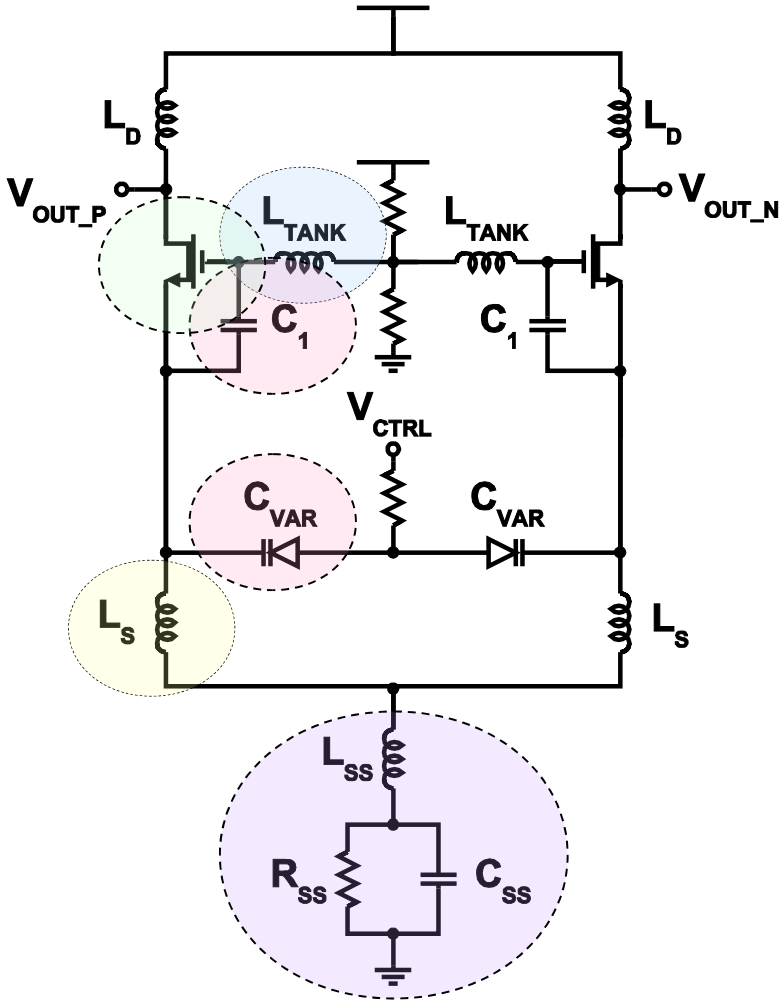
(5) Select $C_1 = C'_1 + C_{gs(be)} >> C_{gs\,(be)}$

$$C_{eq} = C'_{gd} W + \frac{(C'_1 + C'_{gs} W)(C'_2 + C'_{sb} W)}{C'_1 + C'_2 + (C'_{gs} + C'_{sb}) W}$$

$$C_{eq} = C_{bc} + \frac{(C'_1 + C_{be}) C'_2}{C'_1 + C'_2 + C_{be}}$$

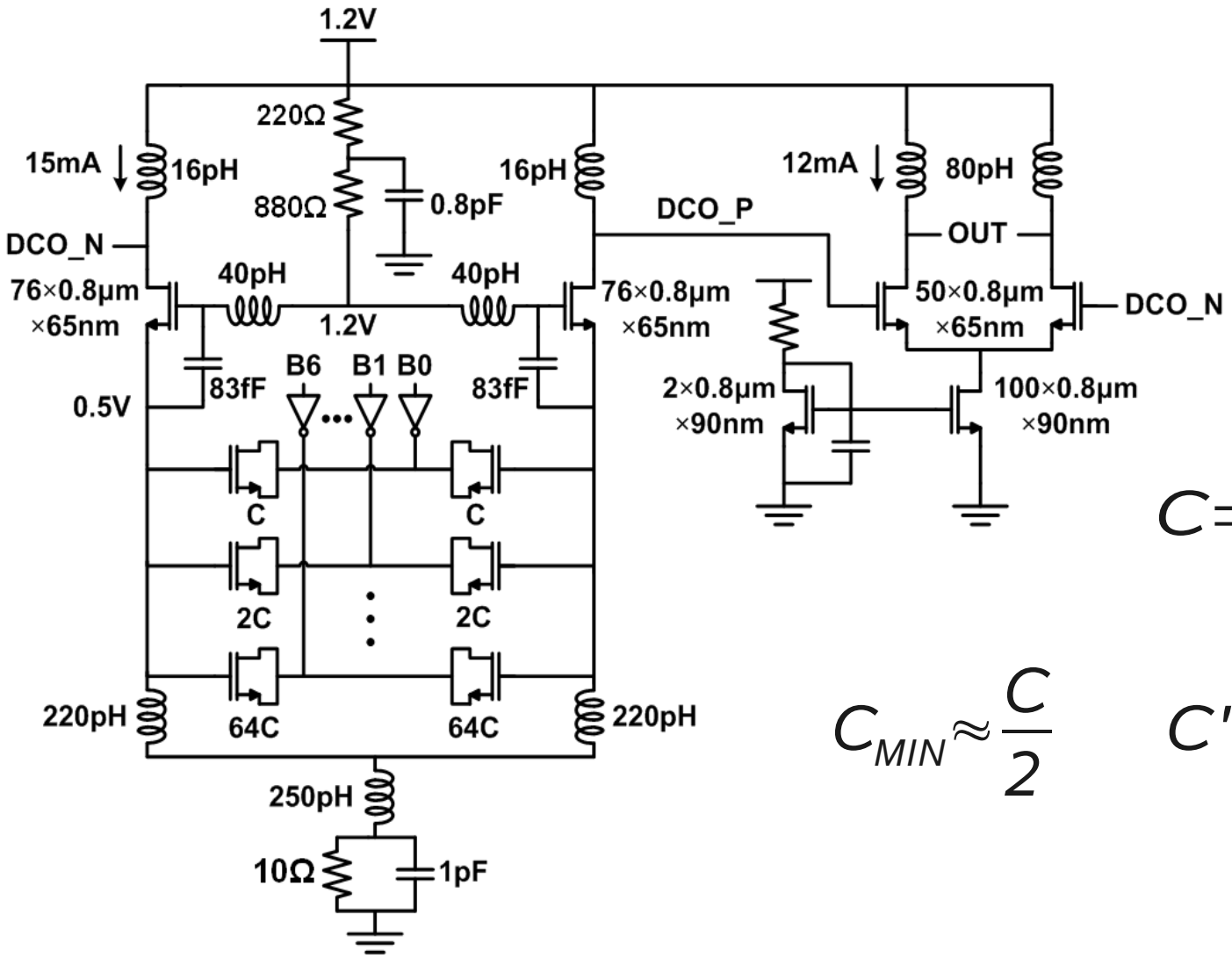
(6) Iterate (3) – (5) to account for layout parasitics.

Colpitts VCO – Design (continued)



- Choose L_S large (AC open)
- Add R_{SS}, C_{SS} and L_{SS} for bias and noise de-coupling
- V_{CTRL} can be digital (DCO)

Design Example: 80-GHz Colpitts DCO



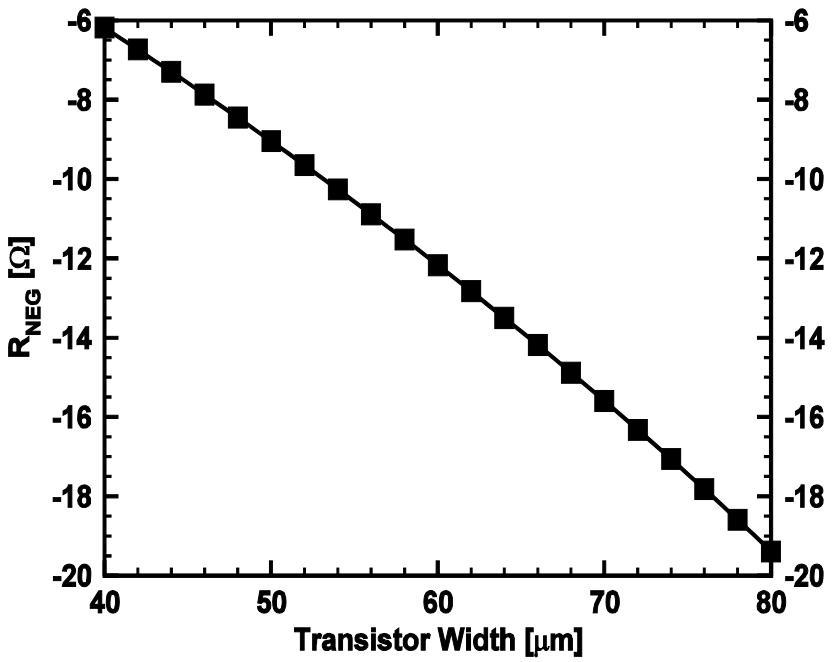
$$C = C'_{ACC} W_{unit}$$

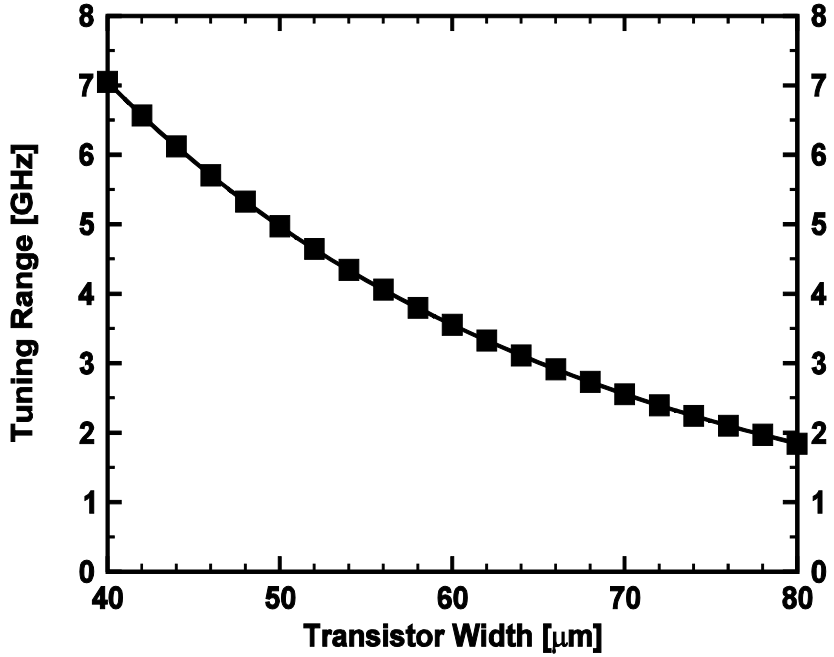
$$C_{MIN} \approx \frac{C}{2} \qquad C'_{ACC} \approx 1.5 \frac{fF}{\mu m}$$

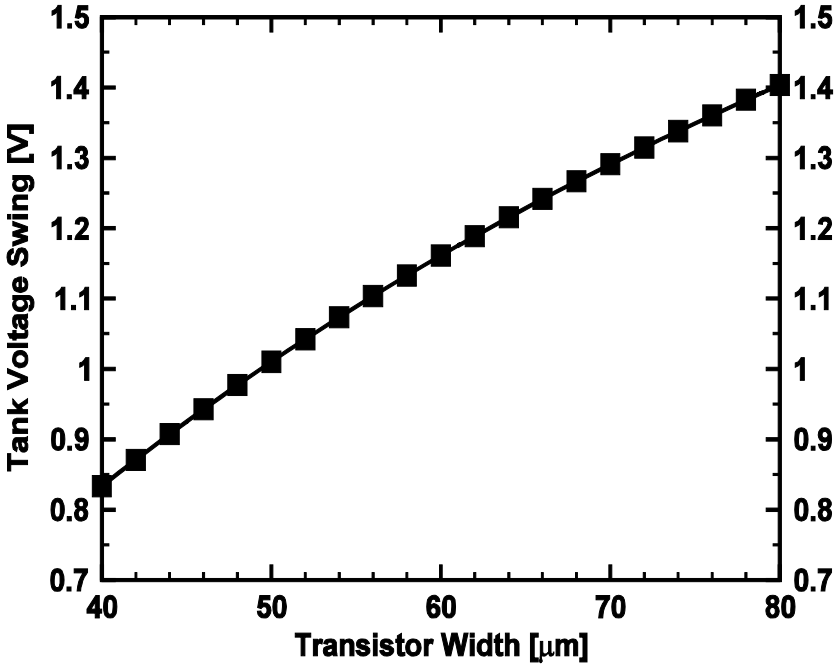
$$C_T = (2^n - 1) C_{MIN} + (C - C_{MIN})(b_0 + b_1 2^1 + b_2 2^2 + \ldots + b_{n-1} 2^{n-1})$$

[M. Khanpour, M.A.Sc. Thesis, Univ. of Toronto, 2008]

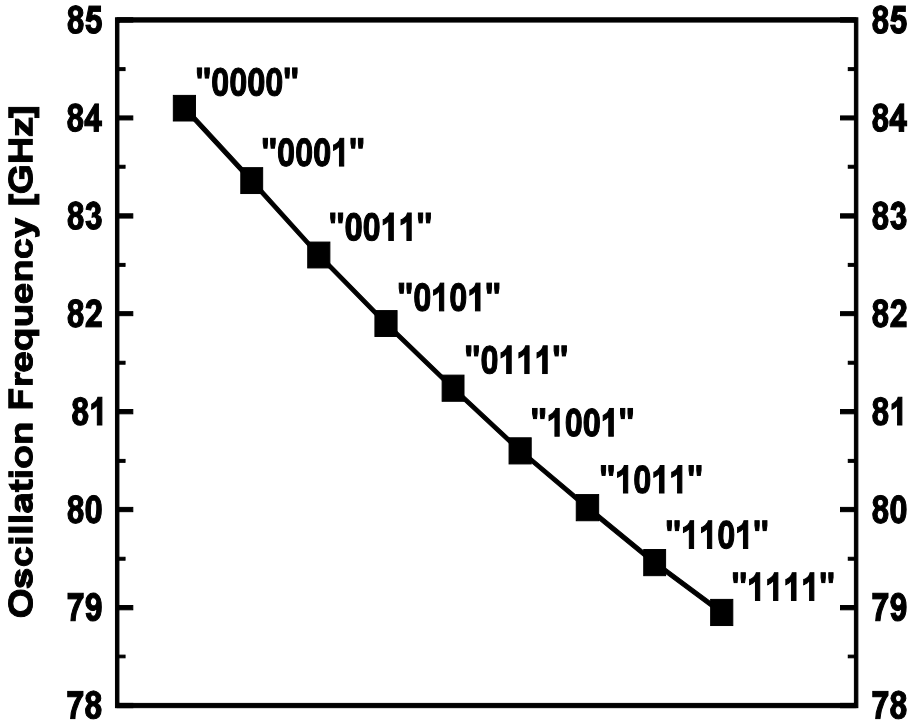
Design optimization

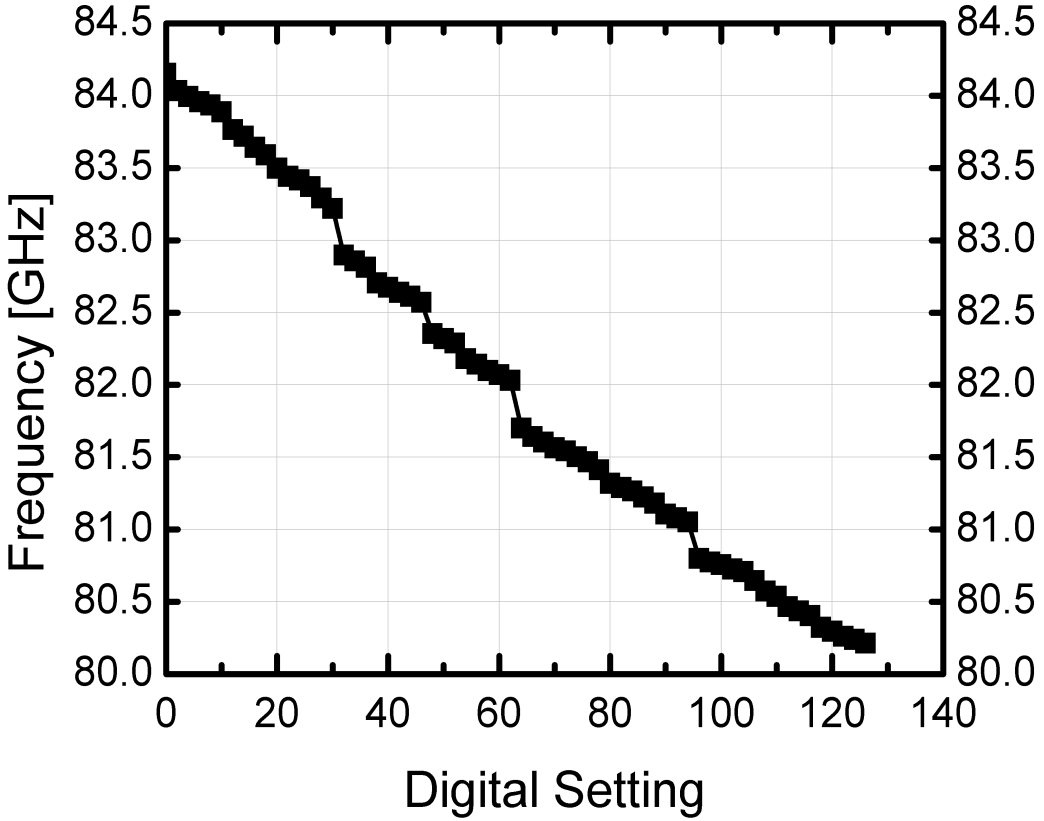






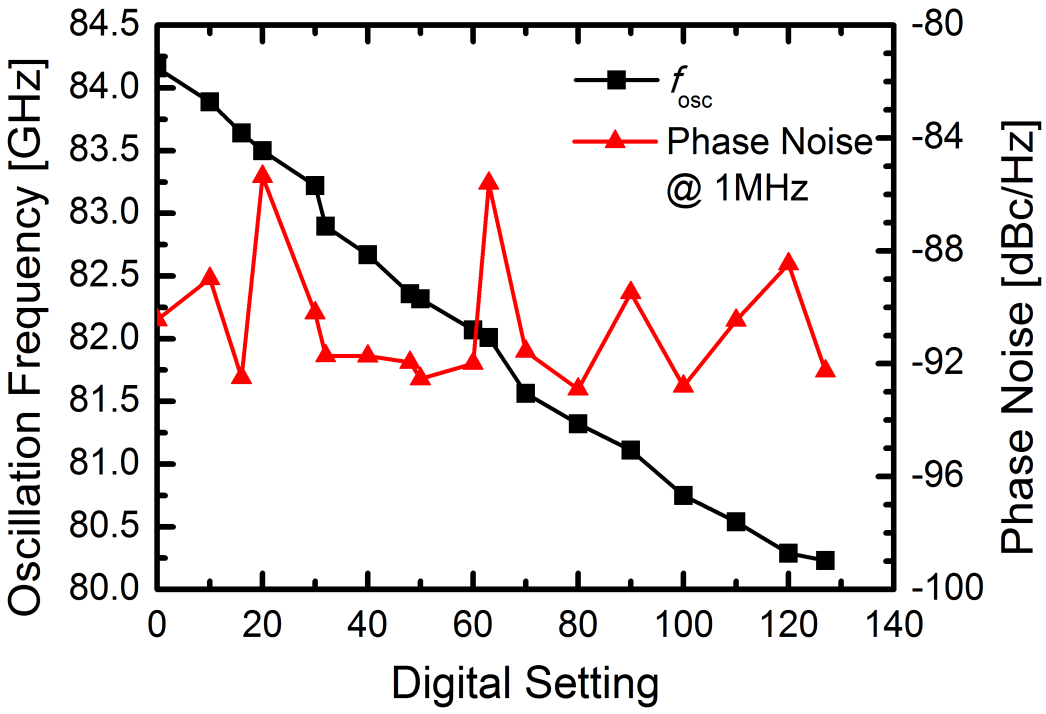
Simulated vs. meas. tuning curve





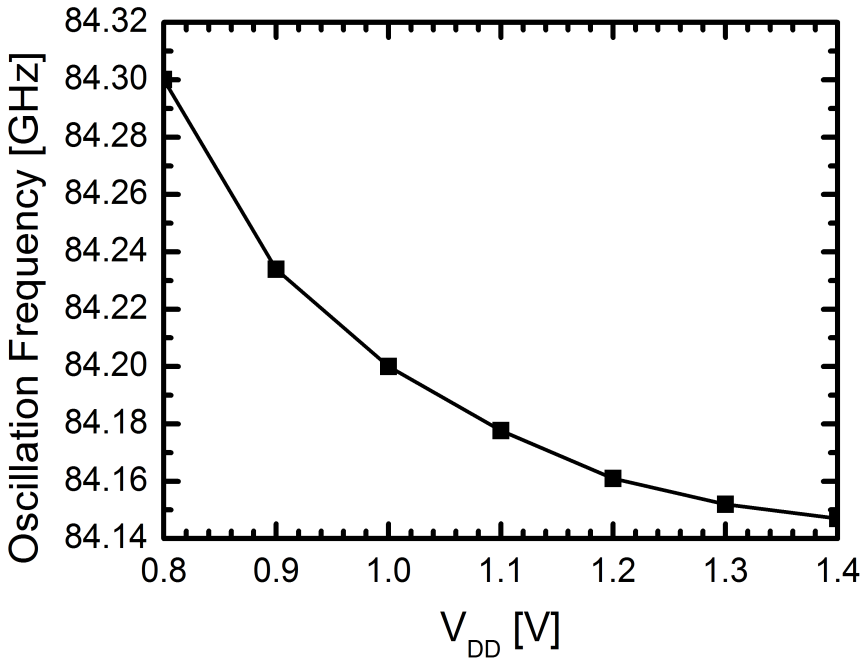
DCO Measurements: PN, Pushing

Phase noise: -85 dBc/Hz to -92 dBc/Hz @1MHz Pushing < 100 MHz/V

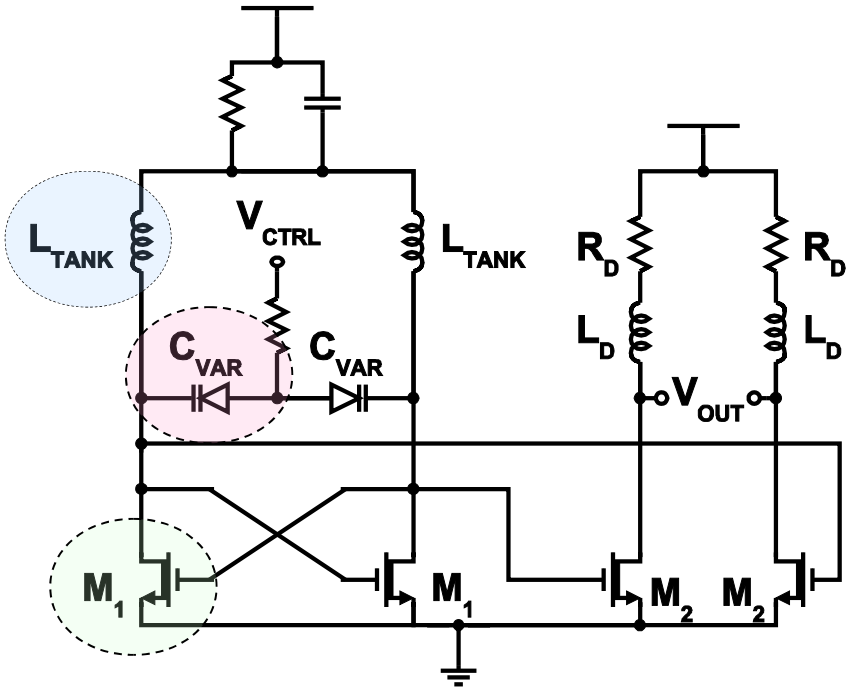


For V_{DD}=1.1-1.3V

Pushing < LSB=31MHz

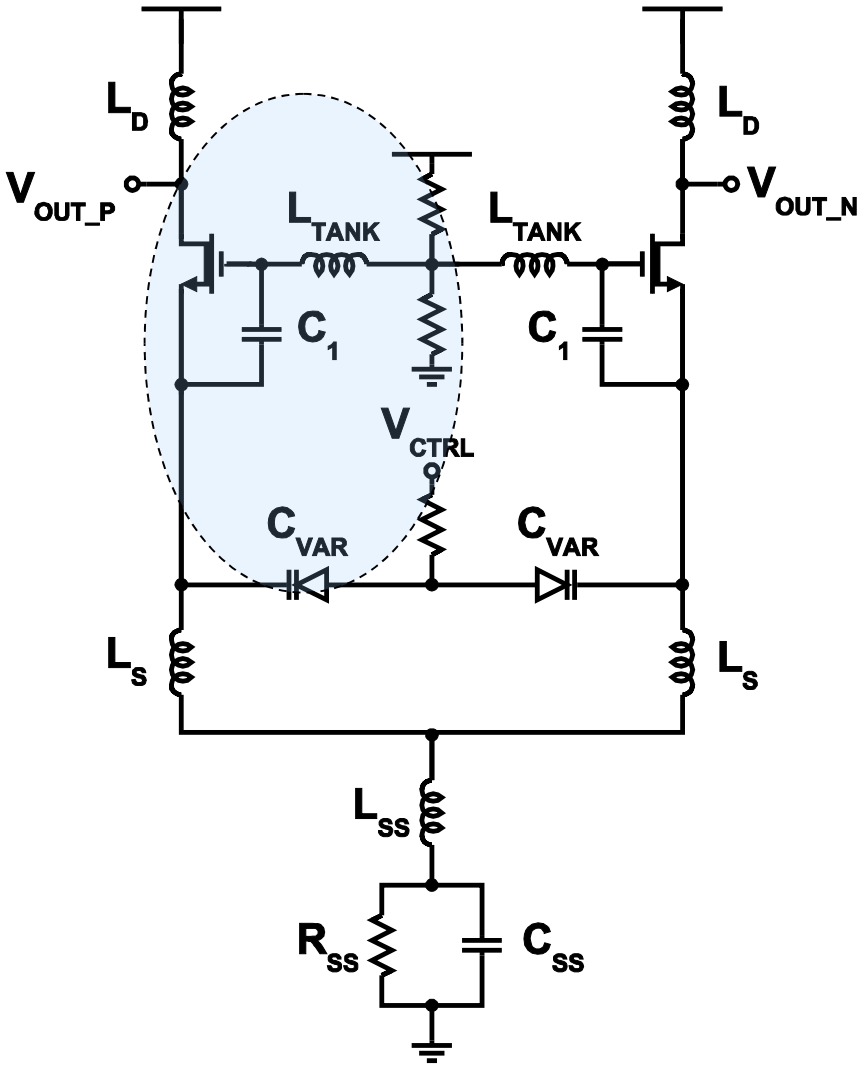


Cross-coupled VCO – Design



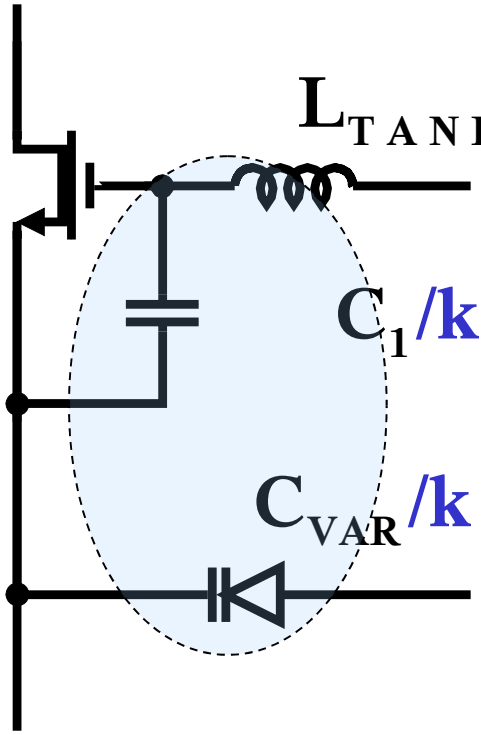
- Choose L_{TANK}
- Bias transistors at optimum noise current density (0.15 mA/µm)
- Size transistors to provide adequate negative resistance
- Calculate C_{VAR} from operating frequency
- Provide buffer to "shelter" tank
- V_{CTRL} can be digital (DCO)

Frequency scaling



$$f_{OSC} \propto \frac{1}{\sqrt{LC}}$$

Frequency Scaling



But...
transistor R-parasitics do not scale since W/k: $(R_s+R_g)\times k$

$\rightarrow k \times f_{osc}$

$$f_{OSC} \propto \frac{1}{\sqrt{LC}}$$

Same applies to cross-coupled VCO

For the same V_{osc}, transistor size and bias current must remain constant

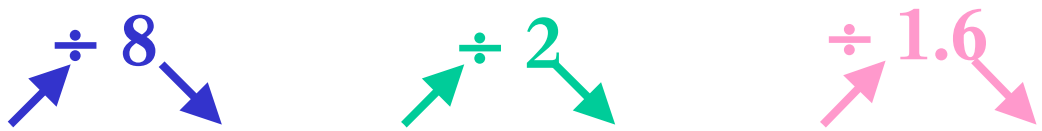
VCO test structures in 180-nm, 90-nm, 65-nm CMOS (digital back-end)

÷ 8 ÷ 2 ÷ 1.6

Colpitts VCO	90-nm 10 GHz	90-nm 80GHz	180-nm 25 GHz	180-nm 50 GHz	90-nm 50 GHz	90-nm 80 GHz	65-nm 80 GHz
L_{TANK} [pH]	435	50	200	100	100	60	40
C_1 [fF]	800	100	100	50	50	35	80
C_{VAR} [fF]	800	100	100	50	50	35	80
W_f [um]	1	1	2	2	2	2	0.8
N_f	100	60	40	20	20	16	76

N_f does not scale with L and C at very high frequency because of parasitic gate and source resistances

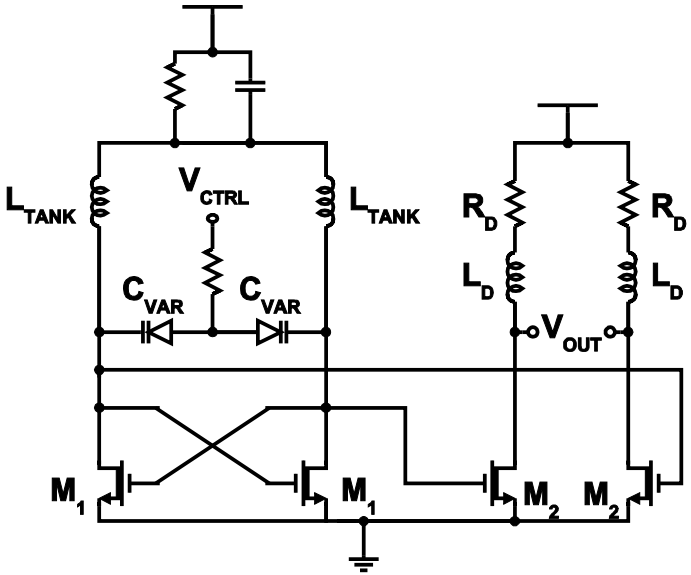
VCO test structures (ii)



Colpitts VCO	90-nm 10 GHz	90-nm 80GHz	180-nm 25 GHz	180-nm 50 GHz	90-nm 50 GHz	90-nm 80 GHz	65-nm 80 GHz
f_{osc} (GHz)	10-12	74-80	23-24.5	49-50.5	49-54	80-85	79-84
W_f (μm)	1	1	2	2	2	2	0.8
P_{DC} (mA)	36	37.5	86.4	57.6	50	37.5	74(32)
P_{OUT}(dBm)	4	-13.6	-1	-9	-12	-17	-3
PN 1MHz	-117.5	-100.3	-98.8	-92.6	-76	-80	-95.7

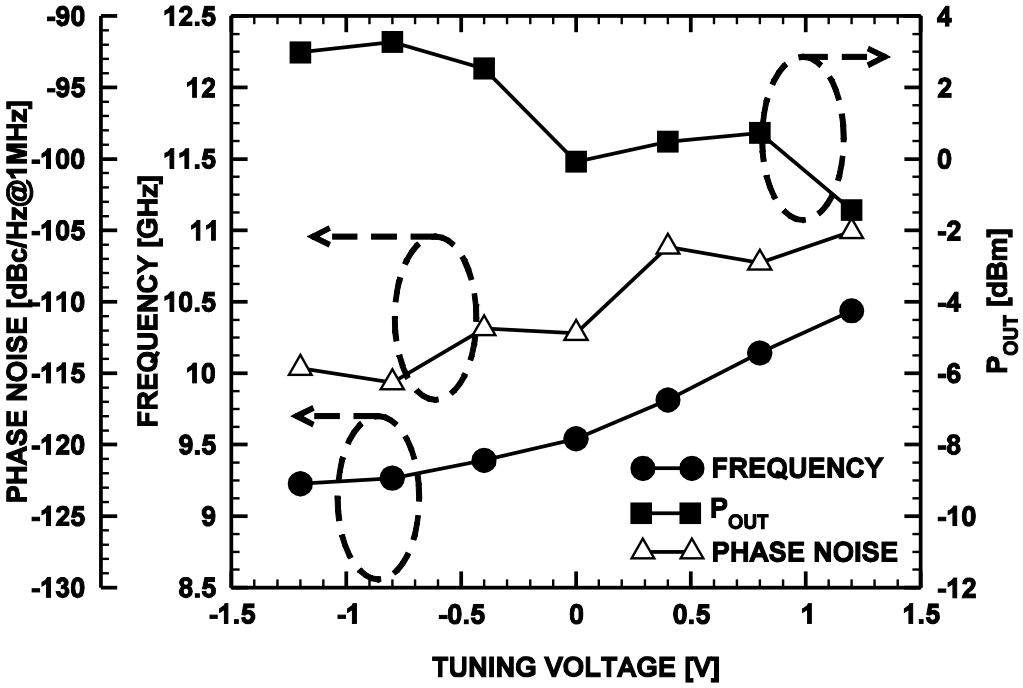
W_f has a dominant impact on phase noise

Cross-coupled VCO test structures



Cross-coupled VCO	90-nm 10 GHz	90-nm 12 GHz	180-nm 17 GHz
L_{TANK} [pH]	435	273	70
C_{VAR} [fF]	260	260	70
W_f [um]	1	1	2
N_f	24	24	40

10-GHz Colpitts VCO



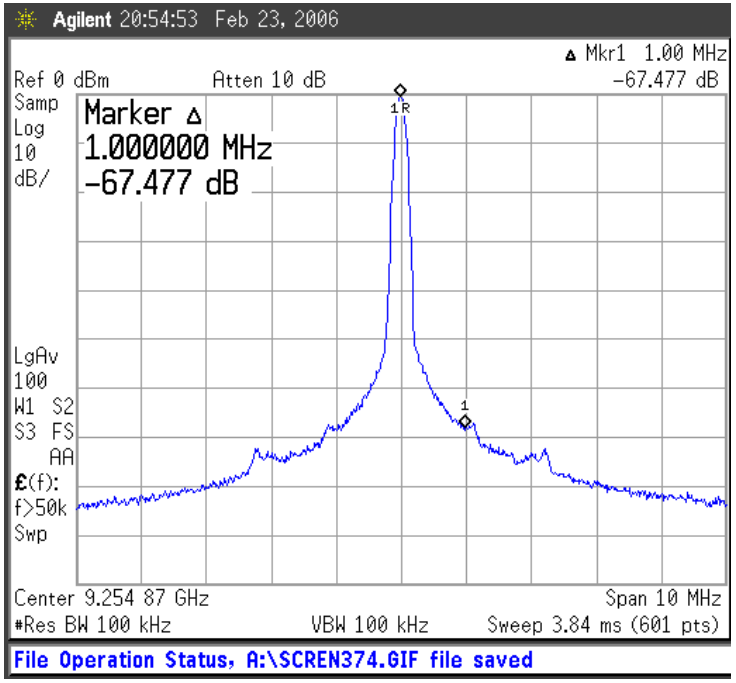
Record phase noise:

-117.5 dBc/Hz @ 1 MHz (100 avg.)

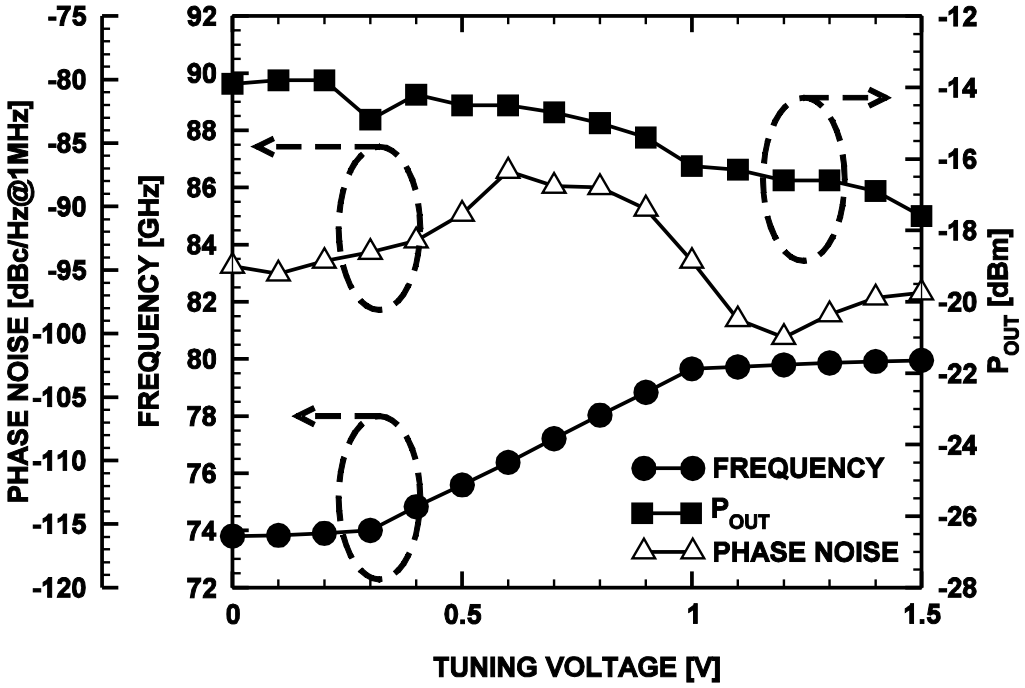
Tuning range:

9.2 – 10.4 GHz

(11.8%)



77-GHz Colpitts VCO



Record tuning range:

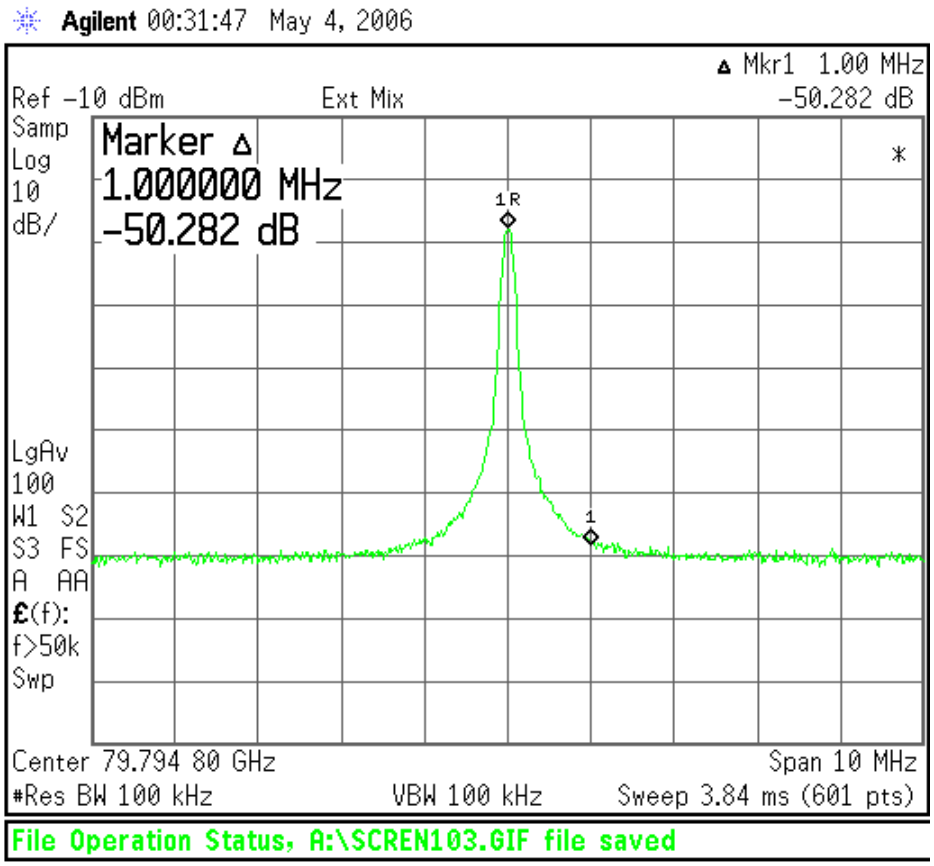
73.8 – 80.0 GHz (8.3%)

Record phase noise:

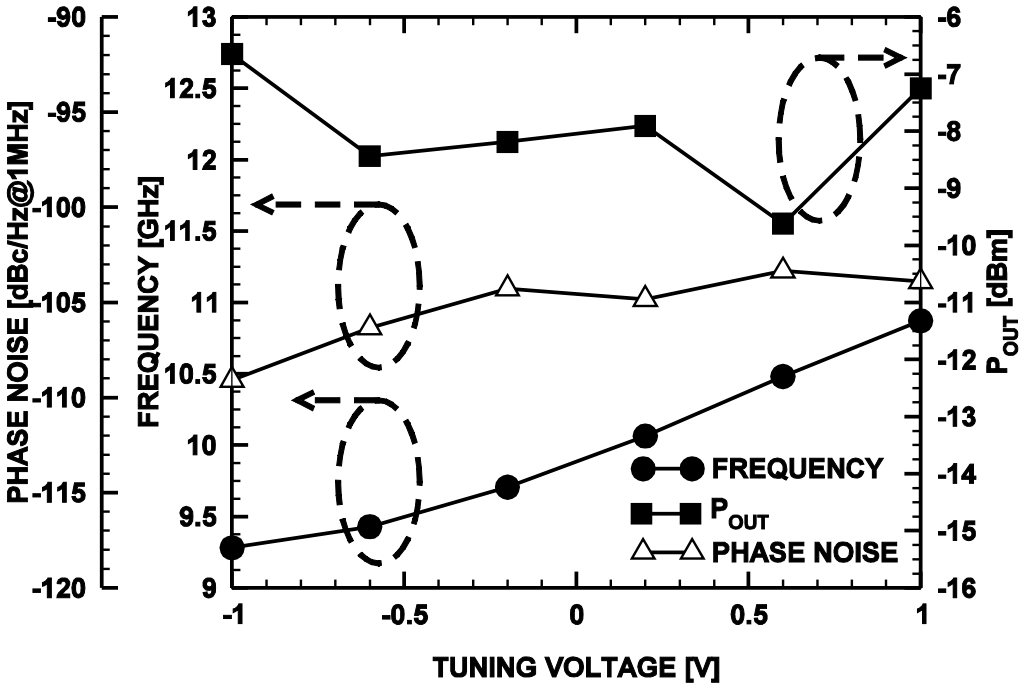
-100.3 dBc/Hz @ 1 MHz (100 avg.)

20log(8) ≈ 17dB higher than

10-GHz VCO's phase noise!



10-GHz Cross-coupled VCO

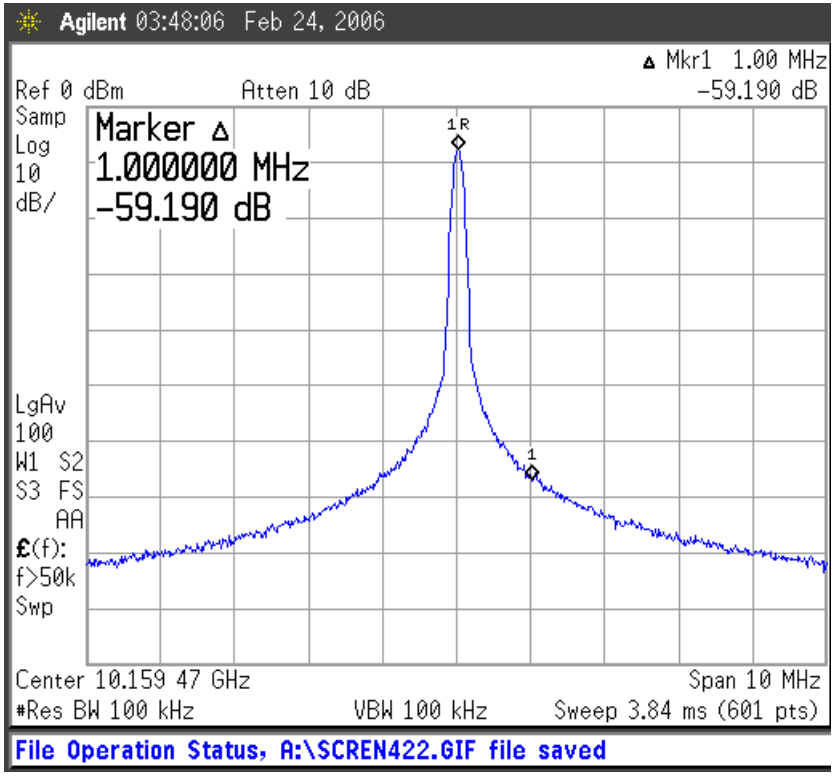


Phase noise:

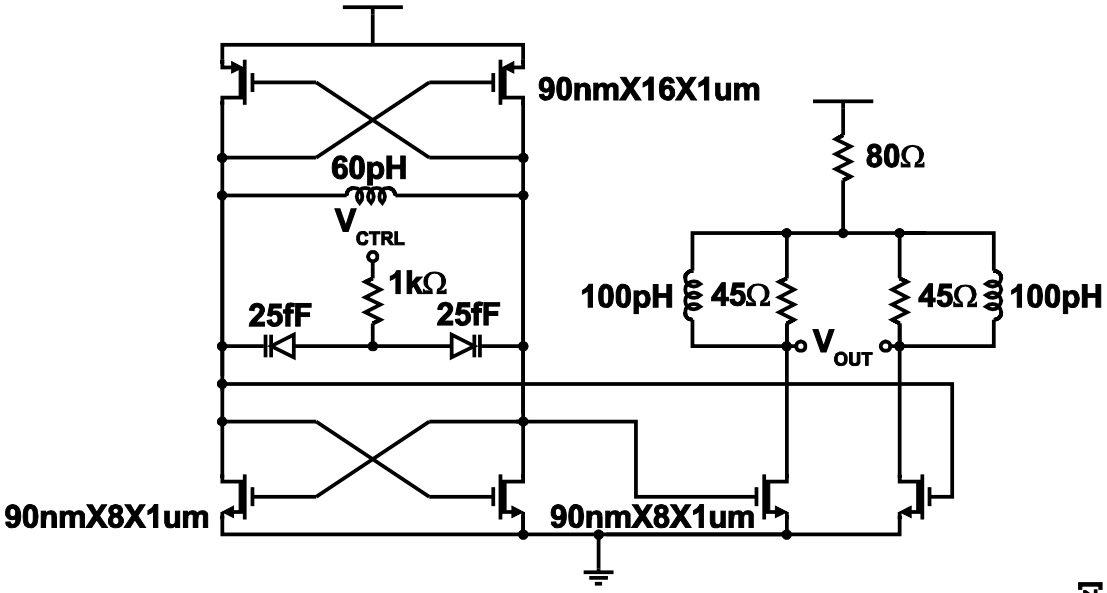
-109.2 dBc/Hz @ 1 MHz (100 avg.)

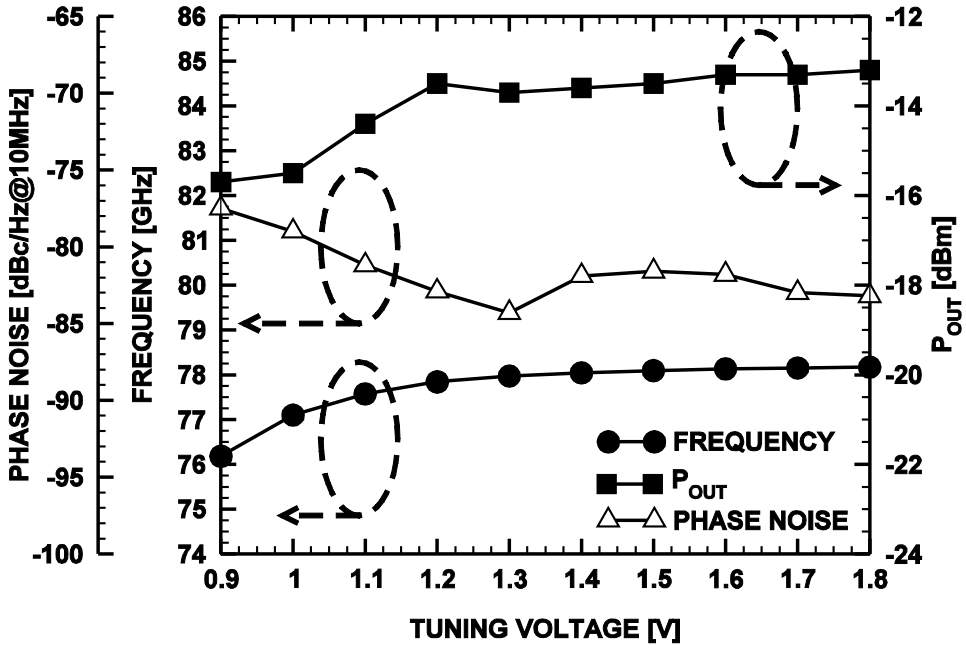
Tuning range:

9.3 – 10.9 GHz (15.8%)



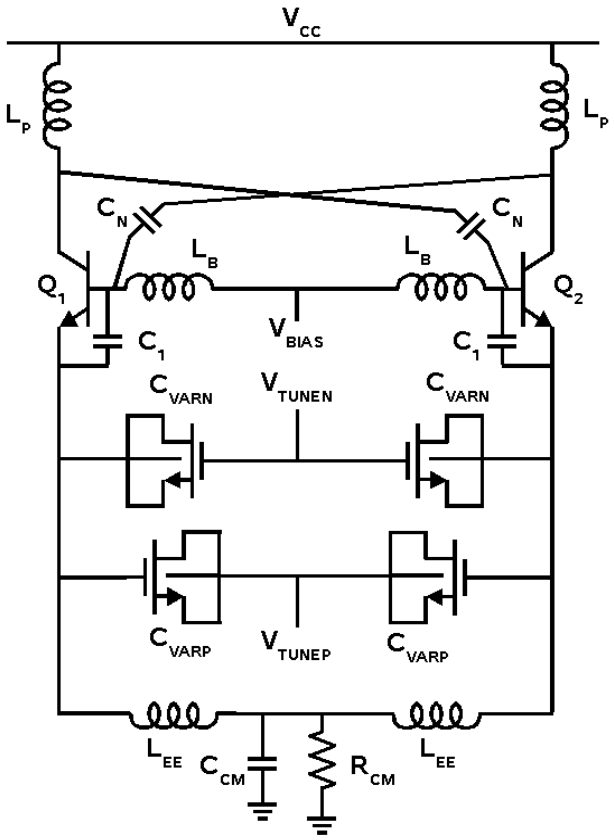
77-GHz 90-nm CMOS cross-coupled VCO





Colpitts VCOs in SiGe BiCMOS and 65-nm CMOS

(S. Nicolson et al. BCTM-2006, E.Laskin et al. ISSCC-2008)



76 GHz, 96 GHz and 104 GHz,

P_{DC}= 120 mW, 2.5V

3% tuning range

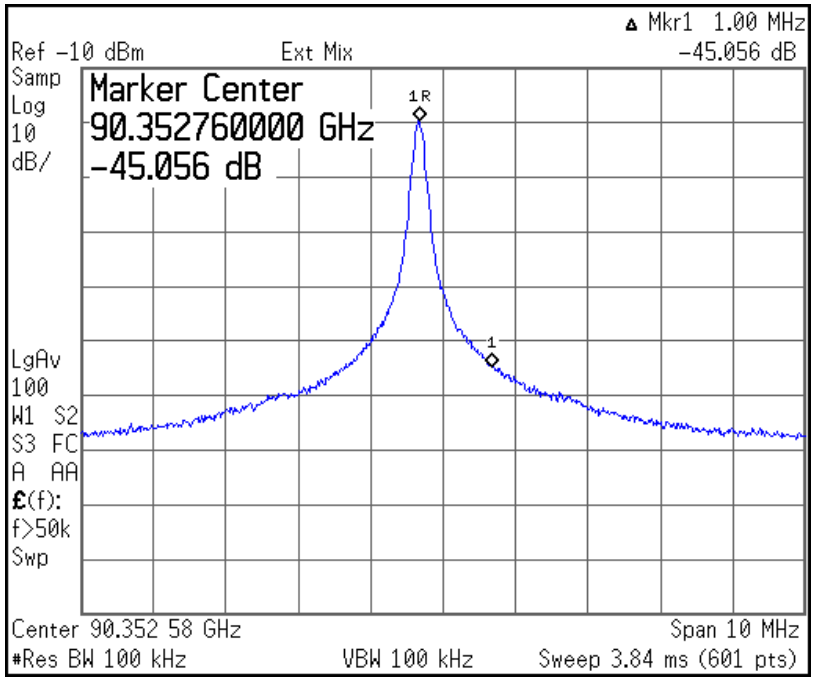
90 GHz, quad + buffers, P_{DC}= 86.4 mW,

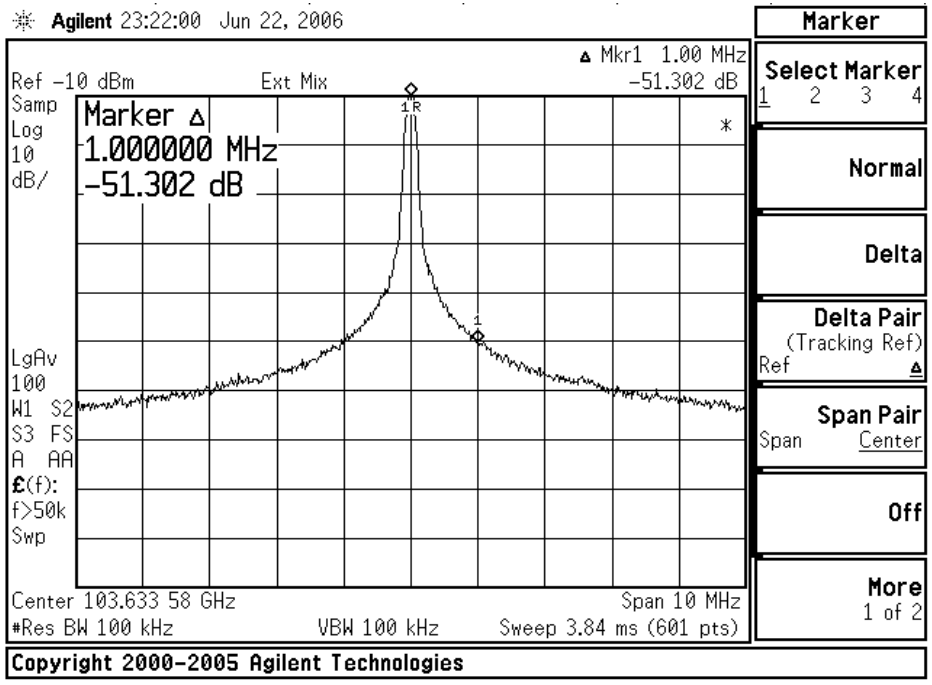
1.2V,

80-GHz DCO, P_{DC}= 60 mW, 1.1V,

3.5%-5% tuning range

90-GHz 65-nm CMOS vs. 104-GHz SiGe HBT Colpitts VCO phase noise





-95 dBc/Hz @ 90 GHz

-101 dBc/Hz @104 GHz

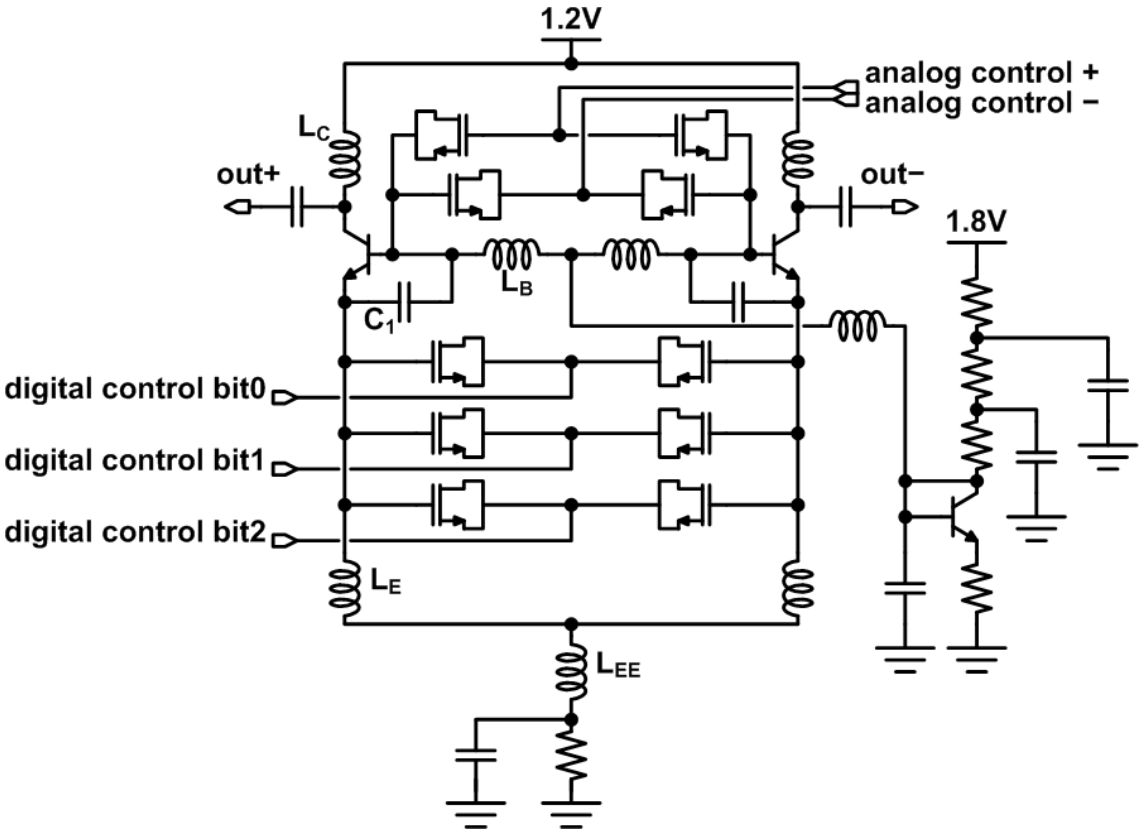
VCO and Buffers

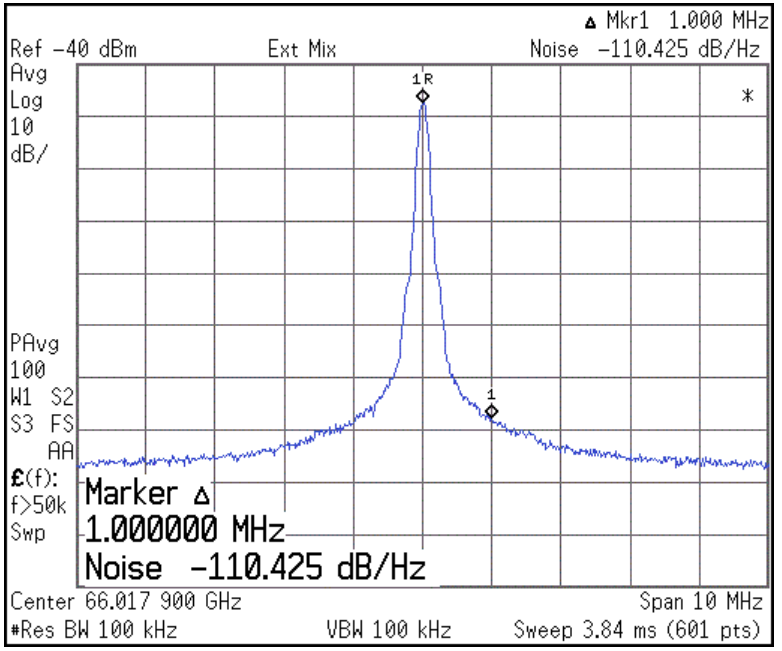
- Symmetry is maintained throughout VCO

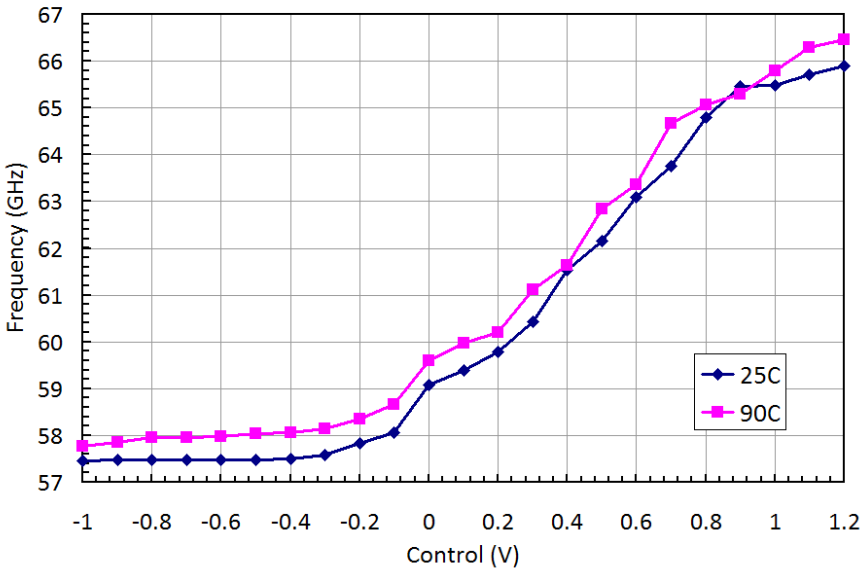
VCO Tuning & Output Power

- 88.2 – 91.2GHz tuning range for all temperatures
- +3dBm to -4dBm total VCO output power

60-GHz Colpitts-Clapp DCO





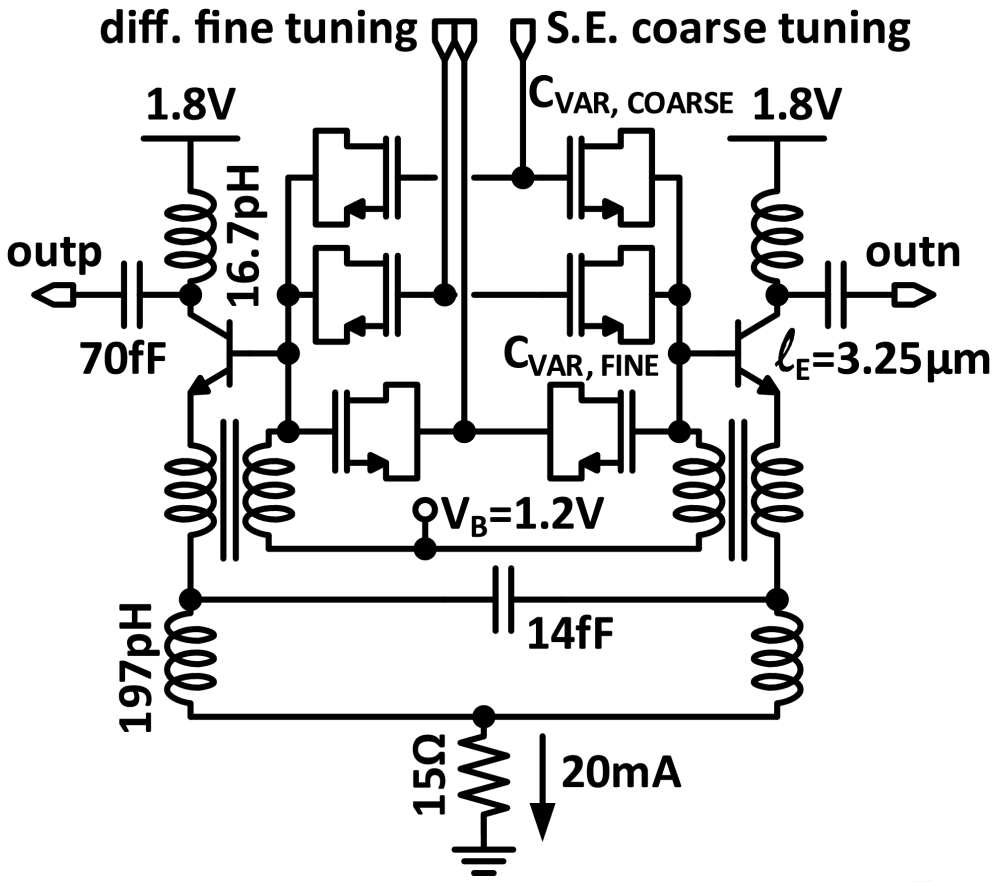


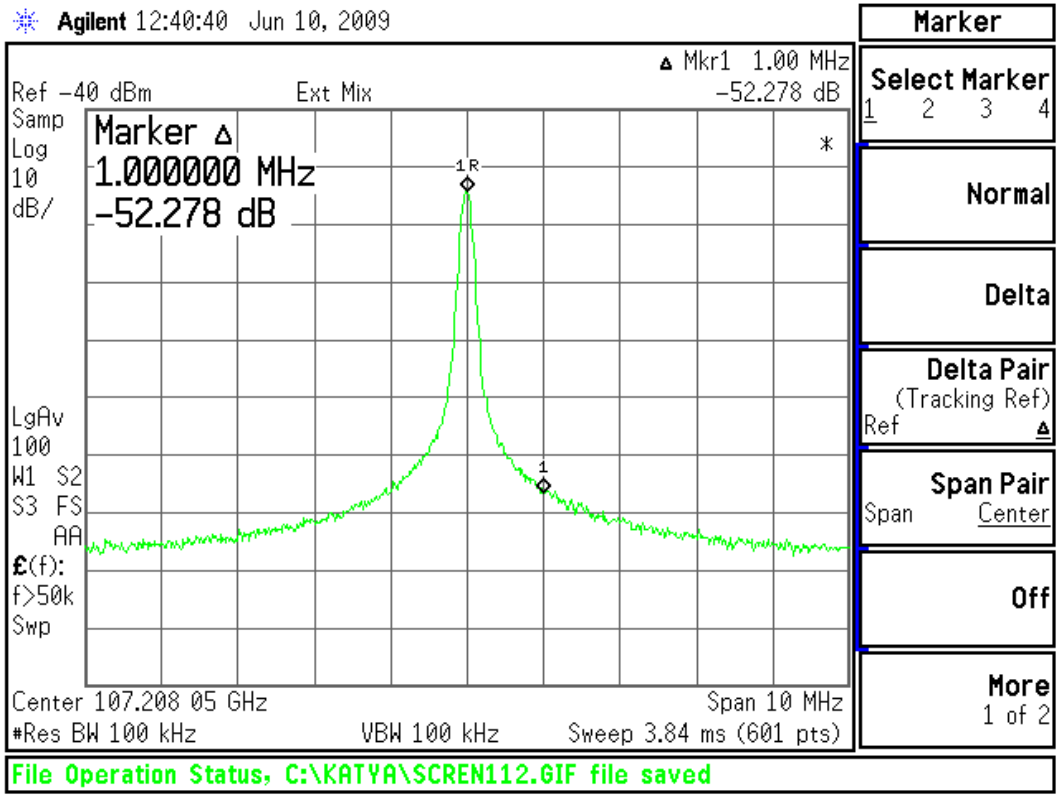
P_{DC}= 25.8 mW, Pout = 3dBm

PN @ 1MHz : -110 dBc/Hz

[E. Laskin et al. RFIC 2011]

110-GHz Armstrong VCO



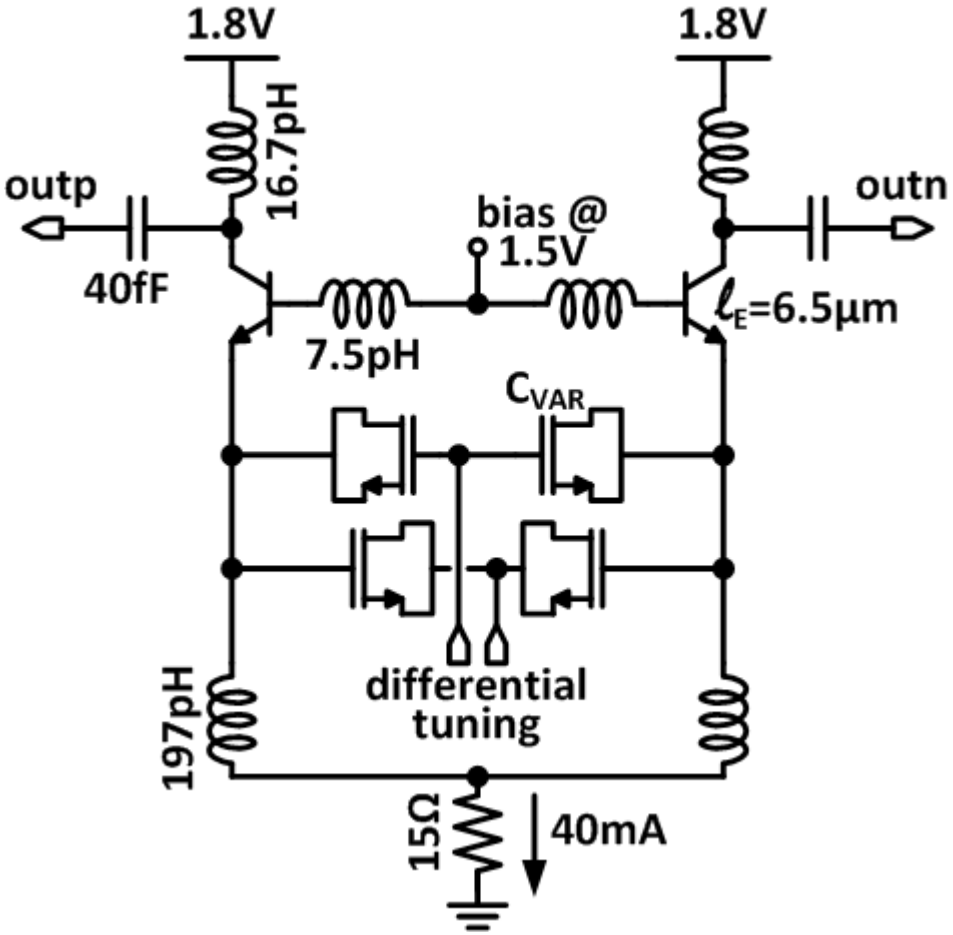


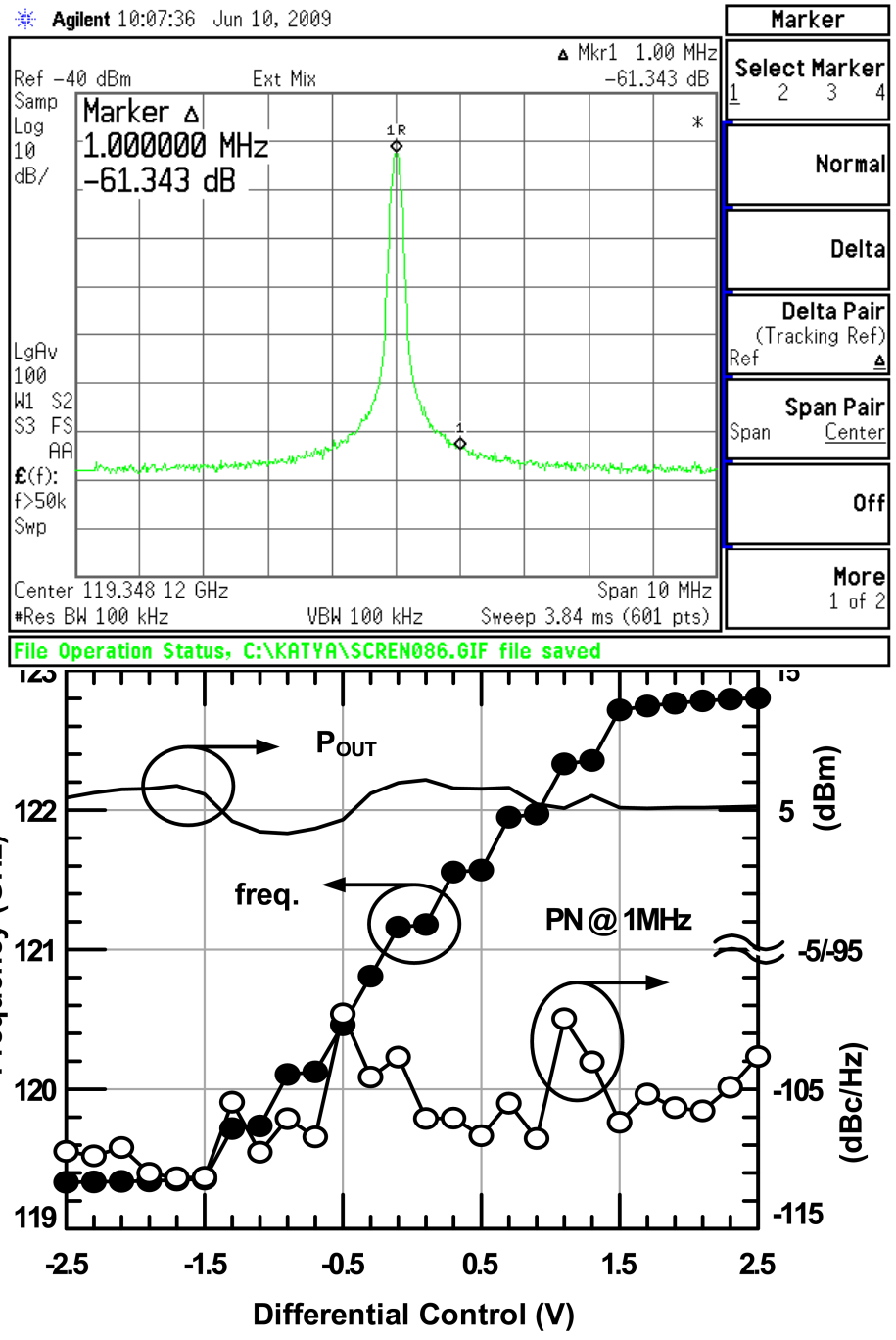
P_{DC}= 36 mW, Pout = 1dBm

PN @ 1MHz : -104 dBc/Hz

E. Laskin, Ph.D. Thesis 2010

120-GHz Colpitts VCO





P_{DC}= 76 mW, Pout = 6dBm

PN @ 1MHz : -111 dBc/Hz

E. Laskin, Ph.D. Thesis 2010

Summary

- VCOs are critical blocks in both radio and optical fiber systems
- VCO design methodology involves a combination of PA and LNA design techniques
- Maximum allowed voltage in a technology is critical in VCOs
- VCOs can be algorithmically scaled in frequency and ported across technology nodes
- Colpitts topology exhibits lower noise and higher output power than cross-coupled topology at mm-wave frequencies