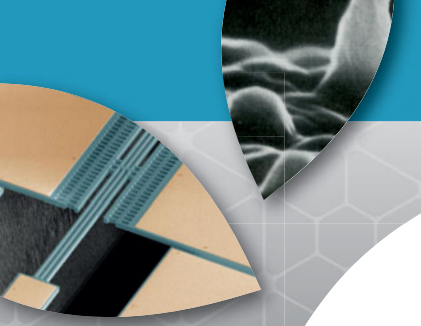

The role of materials science in the evolution of microelectronics

S. Mahajan

This article discusses the role of materials science in the growth and processing of silicon that made modern microelectronics possible. The influence of defects on the electronic properties of silicon is explored, followed by the production of electronic-grade silicon and its conversion into macroscopically dislocation-free doped silicon crystals. The intricacies of dopant distributions in as-grown crystals are also discussed. Oxidation, ion implantation, and metallization are essential elements of device processing, and their salient features are emphasized. The electromigration behavior of interconnects and attempts to prevent it are also introduced.

Introduction

It is no surprise that every leap in human civilization is identified with a material: Stone Age, Bronze Age, Iron Age. The current era is labeled the Information Age, but the designation of Silicon Age might be more appropriate. Indeed, without some of the crucial developments in the synthesis and processing of silicon and related materials, the Information Age might not have materialized.

The existence of semiconductors has been recognized since the time of Michael Faraday in the middle of the 19th century. However, the concept of semiconduction could not be tested because of the lack of availability of high-purity semiconductors. With the advent of zone refining in the mid-1940s, it became possible to purify germanium and silicon to very high levels. This enabled scientists from Bell Telephone Laboratories to demonstrate transistor action in 1948, for which they received the Nobel Prize in Physics in 1956.

In the information technology industry, the principal driving forces for large-scale, very-large-scale, and now ultra-large-scale integration (ULSI) are higher device speeds and reduced costs per chip. These objectives were accomplished by reducing device dimensions and increasing wafer diameters so that the yield of chips per wafer was increased. Because thermal-gradient-induced stresses are the major source of dislocations in as-grown crystals,[1] large-diameter silicon crystals must be grown under precisely tailored thermal gradients. This avoids the multiplication of defect clusters formed by the condensation of point defects during cooling from the melt.[2] These objectives were successfully achieved, and macroscopically dislocation-free silicon crystals as large as 30 cm in diameter are now routinely grown by the Czochralski (CZ) process. The resulting crystals are highly perfect, a crowning achievement of materials engineering.

The as-grown crystals are subsequently sliced into wafers and then polished to remove slicing damage. The polished wafers serve as the platform for the fabrication of ULSI circuits, which entails many steps. **Figure 1** shows a schematic of the well-known metal oxide semiconductor field-effect transistor (MOSFET), one of the building blocks of integrated circuits. In addition, the circuits consist of resistors and inductors, and the various components in a chip are selectively connected to each other by metal interconnects and insulated from each other by dielectrics.

In this article, we review some of the critical challenges that were faced in the realization of ULSI circuits, the silicon-based chips that have driven the information revolution. These challenges included an understanding of electronic properties of defects, growth of highly perfect silicon crystals, development of highly stable dielectrics, localized doping of source and drain regions, and improvement of contacts and interconnects. Lithography is crucial as well for creating ever-finer lateral features, but it is beyond the scope of this article.

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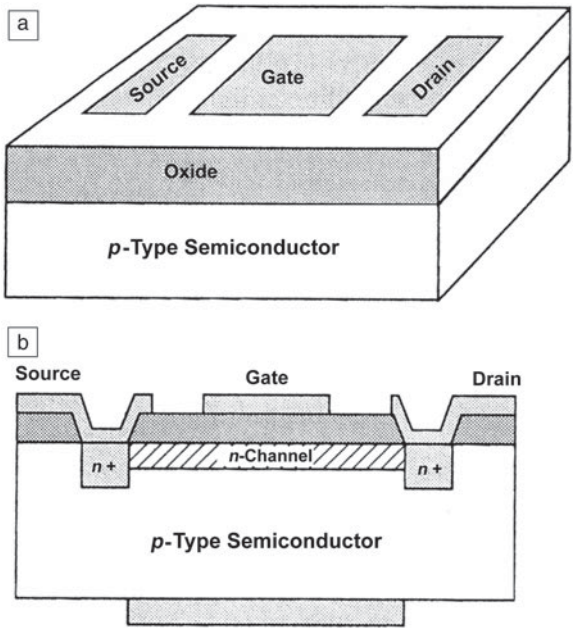

Figure 1. Schematic of the metal oxide semiconductor field-effect transistor structure: (a) top and (b) cross-sectional views of the device. The source and drain contacts are *n*-type ohmic contacts, and the gate is isolated from the channel by an oxide.

Electronic properties of defects in silicon

Using dimensionality as a criterion, defects can be grouped into four categories: zero-, one-, two-, and three-dimensional. Their respective electronic properties differ depending on dimensionality.

Zero-dimensional defects

Silicon has a diamond cubic structure in which each atom is bonded to four others in a tetrahedral arrangement. When a vacancy occurs, each atom constituting a tetrahedron has an unpaired electron. Because unpaired electrons tend to pair, vacancies tend to exhibit acceptor-like behavior. In principle, a distinct energy level within the bandgap should be associated with each pairing, and each energy level must occur at a progressively higher energy because of the electrostatic interactions between the captured electrons. Consequently, a vacancy in silicon can give rise to four distinct energy levels in the bandgap.[3]

The situation regarding interstitials can be addressed in a similar manner. An interstitial has four valence electrons that are not involved in covalent bonding with adjoining atoms. The successive loss of these electrons to the conduction band could, in principle, result in four different levels in the bandgap. Experimentally, a singly ionized donor level at 0.91 eV below the conduction-band edge is seen in silicon.[3]

One-dimensional defects

The introduction of dislocations in silicon, a covalently bonded solid, produces two effects. First, as a result of the elastic distortions associated with a dislocation, band bending occurs in its vicinity. Second, dangling bonds are created along the core of the dislocation.

Many models were proposed to rationalize the electronic properties of dislocations in silicon.[4–7] According to these models, the energy levels associated with a dislocation form a band within the gap. Schröter and Labusch[6] envisaged that, in the neutral state, the band is half-filled. On the other hand, Hirsch[7] suggested that specific energy levels are associated with different dislocation configurations. The application of these models indicates that dislocations behave as acceptors and donors, respectively, in *n*- and *p*-type silicon.

Two-dimensional defects

Because faulted and unfaulted regions are coherently bonded to each other, dangling bonds do not exist at the fault surface. Therefore, intrinsic, extrinsic, and coherent twin boundaries in silicon are not electrically active. On the other hand, partial dislocations bounding various faults are electrically active because of the presence of dangling bonds along the dislocation core.

Sub-boundaries and grain boundaries can be treated as assemblages of dislocations whose Burgers vectors, orientations, and densities depend on the crystallographic characteristics of the boundary. Therefore, the electrical activities of grain boundaries can be analyzed in terms of the electrical behaviors of the dislocations constituting the boundary. To gain additional insight into such analyses, see the review article by Queisser.[8]

Three-dimensional defects

In the case of semicoherent and noncoherent precipitates, dislocations are present at the matrix–precipitate interface. These dislocations can impart electrical activity to these interfaces.

Growth of silicon crystals

Quartzite, a relatively pure form of silicon dioxide, is used in the production of electronic-grade silicon (EGS) that is polycrystalline in nature.[1] The conversion process is carried out in four steps: (1) reduction of quartzite to metallurgical-grade silicon (MGS), which is 98% pure; (2) conversion of MGS into trichlorosilane; (3) purification of trichlorosilane by fractional distillation; and (4) conversion of high-purity trichlorosilane into EGS by chemical vapor deposition.

Currently, only the CZ process, named after its inventor Jan Czochralski, is used for growth of large-diameter silicon crystals. A schematic of a CZ setup is shown in **Figure 2**.[9] EGS serves as the feedstock and is placed in a quartz crucible that is in contact with a graphite susceptor. Melting is achieved by either induction or resistive heating. For doping, there are two options: Either the required amount of dopant is added to the melt, or doped EGS is used.

The loading of EGS into the crucible constitutes the first step in the growth sequence. Then, the growth chamber is evacuated and backfilled with an inert gas, whose function is

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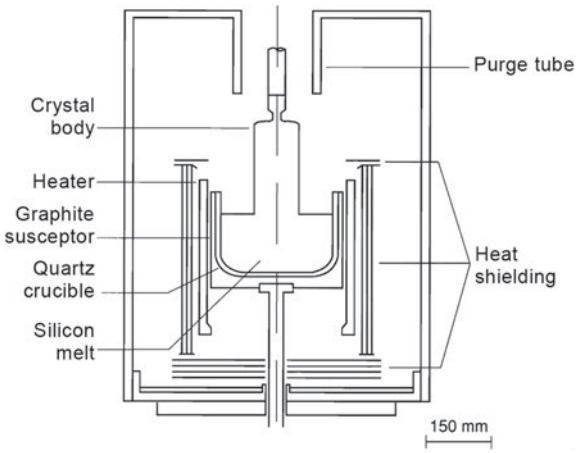

Figure 2. Schematic of the setup used to grow silicon crystals by the Czochralski process. Adapted from Reference 9. © 1992 Pergamon Press.

to prevent oxidation of the melt. Next, a silicon seed of desired orientation, 5 mm in diameter and 100–300 mm in length, is lowered into the molten silicon. The seed is allowed to melt partially and is then withdrawn at a controlled rate. Under the influence of the imposed vertical temperature gradient, the melt solidifies on the seed. The seed serves as a template, and its atomic arrangement is replicated in the newly formed solid. The seed and the crucible are rotated in opposite directions during the pulling process to reduce temperature nonuniformities in the growth system.

The CZ process has one drawback: Because molten silicon is highly reactive, it attacks the quartz crucible, converting silicon dioxide into gaseous silicon monoxide. As the monoxide bubbles through the melt, it dissociates into silicon and oxygen. The released oxygen is incorporated into the as-grown crystals; its concentration is relatively high, ~2×10^{18} atoms/cm^3. Carbon is another contaminant in CZ silicon, and its concentration is in the range of (1–3) × 10^{16}/cm^3. The possible sources for carbon are the starting material, the graphite susceptor, and the heating element.

Sources of dislocations in as-grown crystals

Dislocations in crystals could originate from three different sources: (1) Dislocations present in the seed could propagate into a growing crystal. (2) Excess point defects could cluster together to form dislocation loops during cooling. (3) Under the influence of thermal-gradient-induced stresses, dislocations present in the peripheral regions of a growing crystal could propagate into the interior of the crystal.

Imagine a situation in which dislocations terminate on the seed surface and melt solidifies on the seed. Two distinct possibilities exist: (1) The Burgers vectors of the dislocations are inclined toward the seed surface, or (2) the Burgers vectors of the dislocations are parallel to the seed surface. When the melt freezes epitaxially, dislocations in the first case will be replicated into the newly formed crystals because spiral steps are associated with the emergence points of dislocations at the seed surface. Beam et al.[10] showed that dislocations in the second case will also be replicated because protrusions and depressions are produced where dislocations emerge. Therefore, all of the dislocations present in the seed will be replicated into the as-grown crystal. A cold seed could be thermally shocked when it is dipped in the melt, leading to the multiplication of dislocations. Therefore, two approaches are needed, both to prevent the propagation of dislocations from the seed and to reduce thermal shock. The growth protocols suggested by Dash[11,12] involving small seeds and necking are still being used to produce high-quality crystals.

Doping in the melt

For devices, crystals that have *p*- and *n*-type conductivities and are doped to various levels are needed. These characteristics can be achieved by growing crystals from doped melts. However, there are several factors that complicate the incorporation of dopants into the growing crystals. First, the solubility of an impurity in a melt is generally different from that in a solid, causing continuous changes in the composition of small melts. Second, the externally imposed growth rate might be different from the local growth rate. Third, fluid flow conditions in a growth system are complicated.[1] Finally, the solid–liquid interface might not be planar. In the following discussion, we address the first two challenges, whereas the other two are beyond the scope of the present article.

Crystals having the desired conductivity and a specific carrier concentration can be grown from melts containing appropriate dopant atoms. Even for very high carrier concentrations, extremely small amounts of dopants must be added. Under equilibrium conditions, the concentrations of solute in the solid and the liquid are different because of different solubilities in the two phases. A distribution coefficient under equilibrium conditions, k_{eq}, is defined as

$$k_{eq} = \frac{C_S}{C_L}, \quad (1)$$

where C_S and C_L are the concentrations of solute in the solid and liquid, respectively. Equation 1 assumes that the crystal is growing slowly under equilibrium conditions. The possible values of k_{eq} are greater than 1, less than 1, or equal to 1. The k_{eq} values for some important *n*- and *p*-type dopants and oxygen are listed in **Table I**.

The solute (dopant) concentration near a solid–liquid interface can vary, as illustrated schematically in **Figure 3** for k_{eq} values less than 1. Figure 3a shows crystal growth under equilibrium conditions with a large melt volume. When the melt solidifies, the dopant atoms are rejected into the melt. It can be assumed that these dopant atoms have sufficient time to diffuse away from the solid–liquid interface. Because the melt volume is large, the rejection of dopant atoms into the melt does not change the dopant concentration at the melt–solid interface, namely, C_L.

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Table I. Equilibrium distribution coefficients (k_{eq}) of important impurities in silicon.

Element	Group	k_{eq}
P	VB	3.5×10^{-1}
As	VB	3×10^{-1}
Sb	VB	2.3×10^{-2}
B	IIIB	$\sim 8 \times 10^{-1}$
O	VIB	1.4 ± 0.3

The situation depicted in Figure 3b prevails during the growth of a crystal under steady-state conditions at a finite growth rate. The rejected solute atoms do not have sufficient time to diffuse away from the solid–liquid interface, with the result that the concentration of the dopant builds up at the growth interface to a value, C_O, that is greater than the concentration of solute in the liquid (C_L) in Figure 3a. Assuming that the concentration of the solute in the solid varies linearly with that in the neighboring liquid, the amount of dopant atoms in the solid, namely, C_S, is greater than that incorporated under equilibrium conditions in Figure 3a. The resulting situation can be described using an effective distribution coefficient:

$$k_{\text{eff}} = \frac{C_S^{\text{Nonequilibrium}}}{C_L}, \tag{2}$$

where $C_S^{\text{Nonequilibrium}}$ is the concentration of solute in the solid under nonequilibrium conditions. When k_{eq} is less than 1, k_{eff} is always greater than k_{eq}.

Burton et al.[13] developed the following expression to correlate k_{eff} with k_{eq} and various crystal growth parameters:

$$k_{\text{eff}} = \frac{k_{eq}}{k_{eq} + \left(1 - k_{eq}\right) e^{-f\delta/D}}, \tag{3}$$

where f is the microscopic growth rate, δ is the thickness of the diffusion boundary layer, and D is the diffusion coefficient of the impurity or dopant in the melt. Equation 3 shows that, if f is very high, k_{eff} will approach 1. In general, f differs from the imposed growth rate and depends sensitively on the local growth conditions. As sketched in Figure 3c, if a portion of the crystal freezes at a rate greater than that of the contiguous region, the concentrations of dopant in the two areas will differ, and dopant striations will develop because the crystal is being rotated.

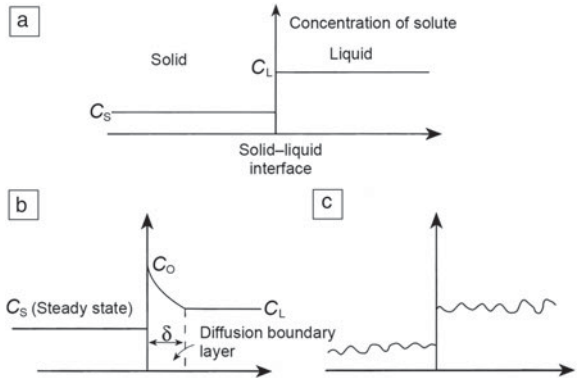

Figure 3. Dopant concentration versus position for possible situations prevailing at the solid–liquid interface during crystal growth: (a) equilibrium growth, (b) finite growth rate for $k_{eq} < 1$, and (c) periodic fluctuations that lead to doping striations.

An interesting question concerns the role of dopant striations in the formation of defect clusters that eliminate the supersaturation of point defects. The x-ray topograph in **Figure 4**, reproduced from the work of de Kock,[14] shows that the impurity striations form a swirl pattern and that defect clusters (labeled A and B) tend to form on the striations; this is not surprising. It was shown later that A clusters are extrinsic dislocation loops bounded by perfect dislocations. Also, these observations seem to suggest that the impurity striations form first and then defect clusters nucleate on them.

Oxygen in CZ silicon

As discussed earlier, as-grown CZ crystals contain $\sim 2 \times 10^{18}$ oxygen atoms/cm^3. This amount represents the solubility limit of oxygen in silicon at the growth temperature and exceeds the solubility limits at the lower temperatures at which silicon devices are processed. Given enough mobility, the dissolved oxygen comes out of solution. We now consider the ramifications of dissolved oxygen on the electrical, structural, and mechanical characteristics of CZ silicon.

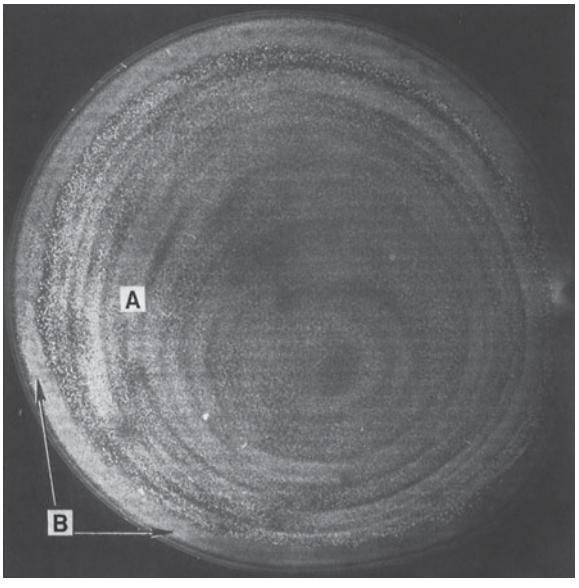

Figure 4. X-ray transmission topograph of a copper-decorated transverse section of silicon crystal. A and B refer to A- and B-type swirl defects. Reproduced with permission from Reference 14. © 1980 North-Holland.

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Electrical characteristics

Oxygen-related thermal donors (TDs) develop in CZ silicon upon annealing at 450°C. TDs have a concentration on the order of $10^{16}/cm^3$ and are electrically active. Energy levels at 0.13 eV and 0.06 eV below the conduction band were observed using Hall measurements.[15] Several investigators, including Oehrlein and Corbett,[16] have attempted to develop models of the structure of TDs that can explain their electrical activity. There is a consensus that TDs consist of silicon and oxygen atoms, but neither the number of oxygen atoms involved nor their spatial distribution is clear.

Structural characteristics

The silicon and oxygen atoms begin to form clusters upon aging. This is not surprising given that the silicon–oxygen bond is very strong. Upon additional aging, clusters can evolve into amorphous or crystalline SiO_2 particles. Because the volume of SiO_2 formed is larger than the volume of silicon consumed in its formation, silicon interstitials must be emitted into the adjoining lattice to accommodate the particles. The question is, what happens to the emitted interstitials? It appears from **Figure 5**, obtained from CZ silicon annealed at 1050°C for 20 h, that the interstitials cluster together to form dislocation loops.[17] Under the influence of precipitate-induced misfit stress, the dislocation loops move away on their glide cylinders. Stacking faults were observed in aged CZ silicon,[18] and their formation could be rationalized in terms of a model proposed by Mahajan et al.[19]

Mechanical properties

It is apparent from the preceding discussion that the precipitation of oxygen during aging of CZ silicon impairs the perfection of the as-grown crystals. The question is whether these impairments have any influence on the mechanical properties of CZ silicon. **Figure 6** shows representative stress–strain curves of crystals deformed at 800°C, 900°C, and 1000°C and also of annealed crystals deformed at 800°C.[20] Significant observations are as follows: (1) The as-grown crystals exhibit a drop in yield at 800°C; the magnitude of the yield drop decreases with increasing deformation temperature, and the drop is absent at 1000°C. (2) The annealed crystals are weaker than the as-grown ones and do not show yield drops. (3) The yield stress exhibits a strong temperature dependence.

Because the as-grown crystals are of high quality, they have few mobile dislocations. When such crystals are deformed, the mobile dislocations have a high velocity because the imposed strain rate, ε*, is related to the number of moving dislocations n and their velocity v by

$$\varepsilon^* = nbv, \tag{4}$$

where b is the magnitude of the Burgers vector. Furthermore, v is given by

$$v = A\tau^m, \tag{5}$$

where A is a material constant, τ is the applied shear stress, and m is the materials exponent. When v is high, τ must be high, that is, the strength of the crystal must be high. However, upon annealing, additional mobile dislocations are introduced into the crystals (i.e., n increases). Therefore, to produce the same strain rate ε*, v must decrease, resulting in a lower value of τ.

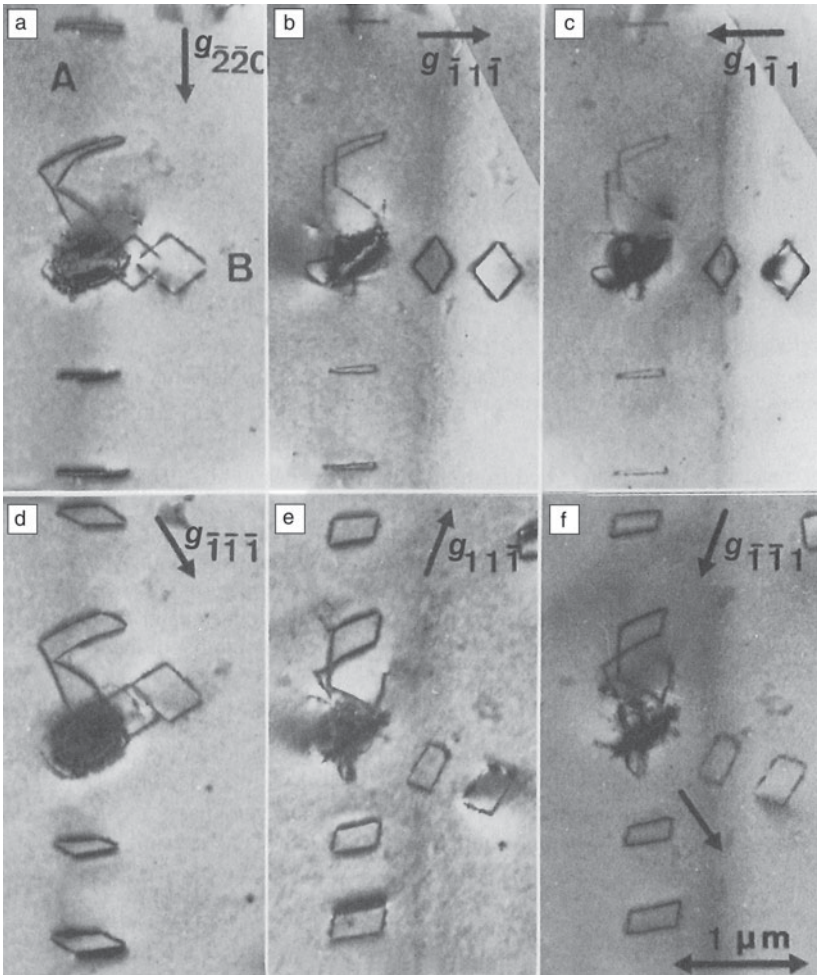

Figure 5. Electron micrographs showing the contrast behavior of prismatically punched-out loops observed in association with plate-like precipitates in CZ silicon annealed at 1050°C for 20 h for different reflections. The different panels show images obtained by selecting different reciprocal-lattice vectors, denoted by g. Reproduced with permission from Reference 17. © 1994 North-Holland.

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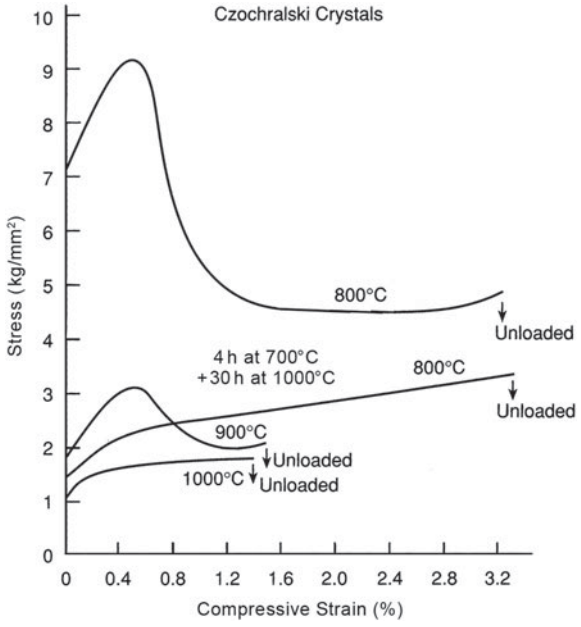

Figure 6. Representative stress–strain curves of CZ crystals, oriented for single slip, at different temperatures. The stress–strain curve of a heat-treated crystal at 800°C is also included. Reproduced with permission from Reference 20. © 1979 Elsevier.

Internal gettering of impurities by silicon–oxygen clusters

As discussed earlier, silicon–oxygen precipitates constitute strain centers. As a result, impurities can segregate to these strain centers. This concept is referred to as impurity gettering,[21] and it has gained considerable acceptance in ULSI technology.

The conditions for internal gettering are created by a two-step annealing process. A high-temperature oxygen out-diffusion anneal is performed first, typically above 1100°C, in a hydrogen atmosphere. During this anneal, the concentration of oxygen in the surface regions where circuit elements are fabricated drops below the solubility limit in the silicon lattice. The first anneal is followed by a low-temperature anneal. During this anneal, silicon–oxygen precipitates form only in the central regions of the wafer where the oxygen concentration is still in excess of the solubility limit. During device processing, impurities can migrate to the strain centers and be eliminated from the regions where circuits are fabricated.

Essential elements of device processing

It is apparent from Figure 1 that the oxide, the lithographically defined source and drain regions, and the associated contacts are essential elements for fabricating a field-effect transistor, the critical component of the modern integrated circuit. Silicon dioxide is an excellent dielectric, and its use is pervasive in silicon technology. Early on, the source and drain regions were defined by diffusion, but now, that approach has been supplanted by ion implantation. Metallization serves two purposes: forming contacts and forming interconnects. In the following discussion, we highlight the salient features of each of these elements.

Oxidation

The ability to produce high-quality SiO_2 films of various thicknesses has played an important role in the evolution of ULSI technology. The SiO_2 film (1) serves as a mask during dopant diffusion or ion implantation for the fabrication of the source and drain regions (see Figure 1), (2) provides electrical isolation between different devices on a chip, (3) is used as a gate oxide and capacitor dielectric in metal oxide semiconductor devices, and (4) provides passivation of silicon surfaces. In addition, SiO_2 layers provide electrical isolation between layers in multilevel metallization schemes.

During the fabrication of integrated circuits, SiO_2 films are formed by the oxidation of silicon at elevated temperatures. Either dry oxygen or steam is used for this purpose. The resulting oxide is stable at subsequent processing temperatures. A linear-parabolic model developed by Deal and Grove[22] can explain most of the experimental data on the growth of SiO_2. In this model, the oxidant is assumed to participate in three serial steps. The first stage involves the transport of the oxidant from the gas phase to the immediate vicinity of the gas–oxide interface. The model assumes that an initial layer of oxide exists on the silicon surface. So, the oxidant moves by diffusion toward silicon, where it reacts with silicon to form an oxide. The resulting oxide is amorphous in nature, and its volume is much larger than the volume of silicon consumed during its formation. Furthermore, stresses develop at the oxide–silicon interface during cooling after oxidation because of the differences in thermal expansion coefficients. The thermal oxidation rates are also affected by the orientation of the silicon surface, the type of dopant in silicon, and the pressure, as well as the presence, of water.

The thermal oxidation of silicon can introduce bowing in wafers, dislocations, and stacking faults. The growth of patterned oxide can lead to substantial local stresses. During oxidation, interstitials are injected into silicon, where they can cluster together to form stacking faults. These faults are electrically active.

The unwanted charges within the oxide and at the silicon–oxide interface have deleterious effects on the performance of devices. According to Deal,[23] four types of charges are associated with the silicon–oxide system: interface-trapped charges, fixed-oxide charges, mobile ionic charges, and oxide-trapped charges. The management of these charges is difficult because our understanding of the silicon–silicon dioxide interface is not optimal.

Over the years, device dimensions have decreased substantially, with the result that the silicon–oxide system is no longer adequate for state-of-the-art devices. Recently, the silicon–oxide system was successfully supplanted by the silicon–hafnium oxide system.

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Ion implantation

Ion implantation refers to a process by which dopant ions having high kinetic energies are introduced into a semiconductor to locally change the carrier concentration and conductivity type; see the source and drain regions in Figure 1. The kinetic energies range between 50 keV and 500 keV for most device applications. Ion implantation is superior to chemical diffusion for selective doping because the lateral diffusion effects are minimal. As a result, implantation has essentially replaced diffusion for selective doping in device processing.

When ions pass through a solid, they collide with nuclei and electrons, thereby losing energy. Eventually, they come to rest in the solid after some distance, which is referred to as the range. The ion paths are not straight and are statistical in nature. As a result, the range can have multiple values. The projection of the range in the implantation direction, called the projected range, is a more meaningful parameter because it determines the junction depth. Assuming that nuclear collisions and Coulomb interactions with the electrons stop incident ions, Lindhard et al.[24] developed a theory for determining the range of an ion.

The concentration profile of implanted ions in an amorphous solid is given by the equation[3]

$$N(x) = \frac{Q_0}{\sqrt{2\pi}\Delta R_p} \exp\left[-\frac{1}{2}\left(\frac{x - R_p}{\Delta R_p}\right)^2\right], \quad (6)$$

where $N(x)$ is the impurity concentration, Q_0 is the dose in ions per square centimeter, x is the distance from the surface in centimeters, R_p is the projected range in centimeters, and ΔR_p is the standard deviation of the projected range (called the straggle) in centimeters. Equation 6 does not include transverse straggle.

Atoms in amorphous solids do not exhibit long-range positional correlations, although short-range correlations might exist. When the ions are incident on such a solid, the probability of the ions encountering atoms within the solid is extremely high. However, this situation does not generally occur with crystalline materials because the presence of long-range three-dimensional atomic arrangements within the crystal creates open channels along certain crystallographic directions. The openness that is observed along a specific direction is referred to as a channel.

Implantations for the fabrication of devices are not carried out under channeling conditions because control of the concentration-versus-depth profiles of the implanted ions would be difficult. To make crystalline solids appear more like amorphous materials to the incident ion beam, the crystal is tilted away from a channeling direction. This approach ensures that the ions do not initially channel.

As indicated earlier, ions undergo nuclear and electronic collisions when they enter the solid. If the energy transferred by the incoming ion to the host lattice atom exceeds a threshold value, called the displacement energy, E_d, the atom will dislodge from its lattice site position. Because the displaced atom can acquire energy in excess of E_d, it can, in turn, displace more atoms from their lattice sites. This process can go on until the energy of the ion falls below E_d. As a result of these multiple collisions, the displacement damage in ion-implanted solids can be quite extensive. The extent of the damage depends on the incident-ion energy, ion dose, dose rate, ion mass, and implantation temperature.

Ion-implantation-induced point-defect damage is extensive. Because the point defects in semiconductors are electrically active, as-implanted materials have poor electrical characteristics. In addition, only a fraction of the implanted ions are located on substitutional sites and contribute to the carrier concentration. To eliminate the detrimental effects of ion implantation, the material has to be annealed at high temperatures. This protocol serves two purposes. First, the point defect density is reduced through mutual annihilation. Second, the implanted dopant atoms in interstitial sites could migrate to lattice sites and become electrically active.

The damage cannot be completely eliminated upon annealing because the distribution of as-implanted damage is statistical in nature. Eaglesham et al. reported "rod-like" defects in silicon implanted with 5×10^{13} ions/cm^2, 40-keV silicon ions and subsequently annealed at 740°C for 15 min.[25] Upon additional annealing, these defects either shrink through the emission of interstitials into the adjoining lattice or coalesce together to form larger ones. Mahajan and Sree Harsha[1] proposed a mechanism for the formation of dislocation networks from these larger loops.

Metallization

Metallization serves two functions in semiconductor technology. Contacts allow an electrical signal to enter into and exit from a device, whereas interconnects provide connections between different devices and passive components on a chip. Contacts are of two types: Schottky and ohmic. The current–voltage characteristics of Schottky contacts are diode-like, similar to those of p–n junctions. On the other hand, the current–voltage characteristics of ohmic contacts are linear over the entire range of voltages and currents to which contacts are subjected; that is, the ohmic contacts interfere least with the incoming and outgoing electrical signals.

Contacts and interconnects in chips are fabricated by selective deposition of metals, alloys, and intermetallics on masked areas. A variety of deposition techniques are currently available for producing such films: physical vapor deposition, sputtering, and chemical vapor deposition.

There are several required characteristics of Schottky contacts: (1) The film must adhere to the semiconductor after deposition, during subsequent device processing, and also in service. (2) The film should not introduce excessive stress in the semiconductor. (3) The Schottky barrier height should be maintained during device operation. The Schottky contacts formed from silicides are more stable than those formed from single metals.

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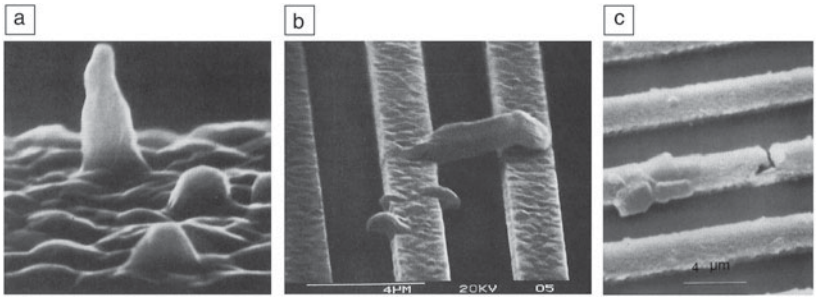

Figure 7. Manifestation of electromigration damage in aluminum films: (a) hillock formation, (b) whisker bridging two conductor lines, and (c) mass accumulation and depletion. Reproduced with permission from Reference 26. © 1980 American Institute of Physics.

The characteristics needed for films for ohmic contacts are similar to those required for Schottky contacts. In addition, the contact resistance should be very low, and the current–voltage characteristics should be linear. In silicon technology, aluminum is used for the formation of ohmic contacts.

In integrated circuits, various components on a chip need to be connected to each other. They are linked to each other using thin conductor lines referred to as interconnects. They are separated from each other and the underlying semiconductor by an insulating layer. Interconnects should be readily depositable, easily patternable with high resolution, and capable of carrying high current densities. Aluminum films satisfy most of these requirements. However, at higher current densities, aluminum interconnects exhibit electromigration, which is mass transport in thin-film conductors under the influence of an electron current. In silicon technology involving aluminum interconnects, electromigration damage is manifested as hillocks on film surfaces (**Figure 7**a), as bridges between two conductor lines (Figure 7b), and as discontinuities in conductor lines (Figure 7c).

The prevention of electromigration in semiconductor technology presents a formidable challenge. The effects on electromigration of different metallurgical variables, including grain size, texture, and alloying, have been explored. It was demonstrated that increasing the grain size, enhancing the 〈111〉 texture, and alloying the aluminum with copper result in improvements in the electromigration resistance.[26] In 1995, an effort was launched to replace aluminum interconnects with copper, and copper interconnects have been successfully incorporated into ULSI technology.

Conclusions

The recent adoptions of alternative gate dielectrics and copper metallization exemplify the continual reinvention of microelectronics to incorporate new materials and processes. Like earlier research on crystalline defects and ion implantation, these advances illustrate the central role that materials science and engineering have played in resolving the critical challenges faced in the development of ULSI technology and the realization of the current silicon-based information age.

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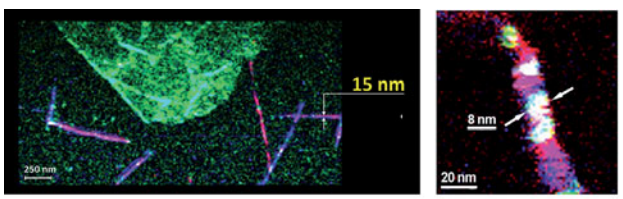

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